NB679GD-Z

MPS,Monolithic Power Systems

Switching Voltage Regulators 26V Fixed 5V-8A Sync Buck Converter

The Future of Analog IC Technology®

NB679

28V, Low Iq, High Current, Fixed 5V-8A Synchronous Buck Converter with 100 mA LDO

DESCRIPTION

The NB679 is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with a fixed 5 V output. It offers a very compact solution to achieve 8 A continuous output current and 10 A peak output current over a wide input supply range with excellent load and line regulation.

The NB679 operates at high efficiency over a wide output current load range based on MPS proprietary switching loss reduction technology and internal low Ron power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

NB679 provides a fixed 5 V LDO, which can be used to power the external peripheries.

Full protection features include OC limit, OVP, UVP, and thermal shutdown.

The converter requires a minimum number of external components and is available in QFN 2mm x 3mm package.

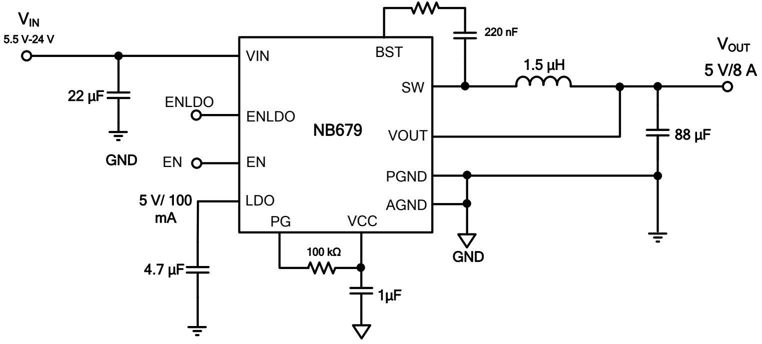
FEATURES

- Wide 5.5 V to 28 V Operating Input Range
- Fixed 5 V Vout
- Supports 5.5 V-5 V
- Ultrasonic Mode with Fs over 25 kHz
- 100 μA Low Quiescent Current
- 8 A Continous Output Current
- 10 A Peak Output Current
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop for Load Regulation
- Stable with POSCAP and Ceramic Output Capacitors
- Built-In 5 V, 100 mA LDO with Switch Over
- 1% Reference Voltage
- Internal Soft Start
- Output Discharge
- 700 kHZ Switching Frequency
- OCP, OVP, UVP, and Thermal Shutdown.
- Latch-Off Reset via EN or Power Cycle
- QFN-12 (2mm x 3mm) Package

APPLICATIONS

- Laptop Computers
- Tablet PCs
- Networking Systems
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
NB679GD	QFN-12 (2mm x 3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. NB679GD–Z)

TOP MARKING

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ALTY
 LLL
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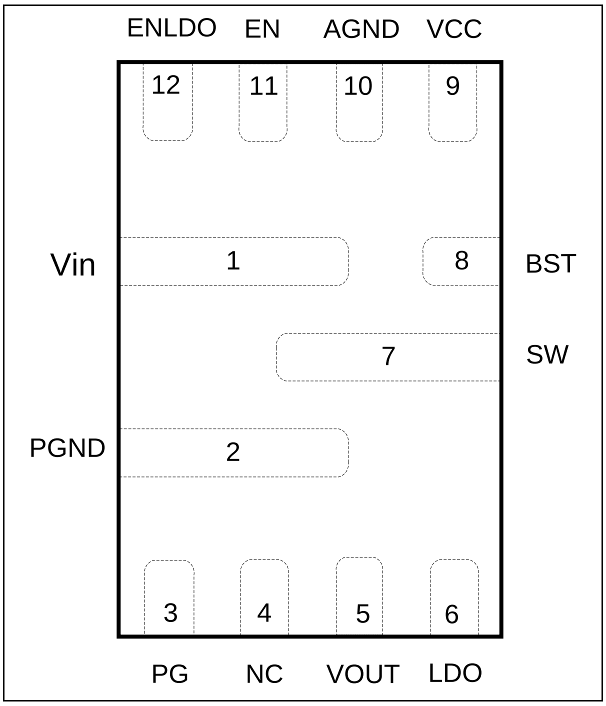
ALT: Product code of NB679GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN})	28 V
V_{SW} (DC)	-1 V to 26 V
V_{SW} (25 ns)	-3.6 V to 28 V
V_{BST}	V_{SW} +4.5 V
V_{OUT},V_{LDO}	-0.3 V to 6.5 V
All other pins	-0.3 V to +4.5 V
Continuous power dissipation (T_A=+25°C) (2)	
QFN-12 (2mm x 3mm)	1.8 W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage	5.5 V to 24 V
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-12 (2mm x 3mm)	70	15	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0 V, V_{ENLDO} = 0 V,		1	2	μA
Supply current (quiescent)	I_{IN}	V_{EN} = V_{ENLDO} = 3.3 V, V_{OUT} = 5.5 V		110	130	μA
Supply current (standby)	I_{IN}	V_{EN} = 0 V, V_{ENLDO} = 3.3 V, I_{LDO} = 0 A		60	80	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			25		mΩ
Low-side switch on resistance	LS_{RDS-ON}			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0 V, V_{SW} = 0 V		0	1	μA
Current limit						
Low-side valley current limit	I_{LIMIT}		10	11	12	A
Switching frequency and timer						
Switching frequency	F_S			700		kHz
Constant on timer	Ton	Vin = 10 V	600	710	820	ns
Minimum on time(6)	$T_{ON\ Min}$			50		ns
Minimum off time(6)	$T_{OFF\ Min}$			220		ns
Ultrasonic mode						
Ultrasonic mode operation period	T_{USM}		20	30	40	μs
Over-voltage and under-voltage protection						
OVP threshold	V_{OVP}		117%	122%	127%	V_{REF}
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-1 foldback timer(6)	T_{UVP-1}			32		μs
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and soft start						
Vout REF voltage	$V_{OUT\ REF}$		4.95	5	5.05	V
Soft-start time	T_{SS}	EN to Vout OK		1.7	2.5	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
EN rising threshold	$V_{EN\ H}$		1.2	1.3	1.4	V
EN hysteresis	V_{EN-HYS}			150		mV
ENLDO rising threshold	$V_{EN\ H}$		1.2	1.3	1.4	V
ENLDO hysteresis	V_{EN-HYS}			150		mV
EN high limit @ USM	$V_{EN\ H\ USM}$				1.8	V
EN low limit @ normal	$V_{EN\ L\ Normal}$		2.6			V
EN input current	I_{EN}	V_{EN} = 2 V		5		µA
		V_{EN} = 0 V		0		
VIN under-voltage lockout threshold rising	VIN_{VTH}			4.45	4.7	V
VIN under-voltage lockout threshold hysteresis	VIN_{HYS}			450		mV
LDO regulator						
LDO regulator	V_{LDO}	V_{EN} = 0 V	4.85	4.97	5.12	V
LDO load regulation		V_{EN} = 0 V, LDO load =100 mA		2		%
LDO limit$^{(5)}$	$I_{LDO\ Limit}$	V_{EN} = 0 V, V_{LDO} = 4.5 V		135		mA
Switch Rdson$^{(5)}$	R_{Switch}	I_{LDO} = 50 mA		0.9	1.2	Ω
VCC regulator						
VCC regulator	V_{CC}		3.5	3.6	3.7	V
VCC load regulation		Icc = 5 mA		5		%
Power good						
PG when FB rising (good)	$PG_{Rising(Good)}$	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB falling (fault)	$PG_{Falling(Fault)}$	V_{FB} falling, percentage of V_{FB}		85		
PG when FB rising (fault)	$PG_{Rising(Fault)}$	V_{FB} rising, percentage of V_{FB}		115		
PG when FB falling (good)	$PG_{Falling(Good)}$	V_{FB} falling, percentage of V_{FB}		105		
Power good low to high delay	PG_{Td}			750		µs
EN low to power good low delay	$PG_{Td\ EN\ low}$				5	µs
Power good sink current capability	V_{PG}	Sink 4 mA			0.4	V
Power good leakage current	$I_{PG\ LEAK}$	V_{PG} = 3.3 V			5	µA
Thermal protection						
Thermal shutdown$^{(5)}$	T_{SD}			140		°C
Thermal shutdown hysteresis$^{(5)}$	T_{SD-HYS}			25		°C

NOTE:

5) Guaranteed by design.

PIN FUNCTIONS

NB679

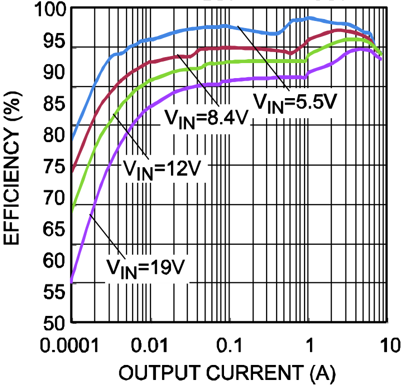
PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulator. The NB679 operates from a 5.5 V to 24 V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for this input trace.
2	PGND	**Power ground.** Use wide PCB traces and enough vias to handle the load current to make the connection. Make the PGND trace to the Vin decoupling capacitor as wide as possible.
3	PG	**Power good output.** The output of PG is an open-drain signal. It is high if the output voltage is higher than 95 percent of the nominal voltage or lower than 105 percent of the nominal voltage.
4	NC	**No connection.**
5	VOUT	**VOUT is used to sense the output voltage of the buck regulator**. Connect VOUT to the output capacitor of the regulator directly. Also, VOUT acts as the input of the internal LDO switch over power input. Keep the VOUT sensing trace far away from the SW node. Avoid vias on the VOUT sensing trace. A >25 mil trace is required.
6	LDO	**Internal LDO output.** Decouple with a minimum 4.7 µF ceramic capacitor as close to LDO as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. If ENLDO is high, it switches over to the LDO to buck after PG is ok.
7	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW negative during the off-time. The on-resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection. Try to minimize the area of the SW pattern.
8	BST	**Bootstrap**. A capacitor connected between SW and BS is required to form a floating supply across the high-side switch driver.
9	VCC	**Internal VCC LDO output**. The driver and control circuits are powered from this voltage. Decouple with a minimum 1 µF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
10	AGND	**Signal logic ground.** Kelvin connection to PGND.
11	EN	**Buck enable.** EN is a digital input that turns the buck regulator on or off. When the power supply of the control circuit is ready, drive EN high to turn on the buck regulator, and drive it low to turn off the buck regulator. Connect EN to 3V3 through a pull-up resistor or a resistive voltage divider for automatic start-up. Do NOT float this pin. EN can be used to set USM. When EN is in the range of 1.4 V to 1.8 V, it enters USM. If EN is in the range of 2.6V to 3.6V, it operates in normal mode.
12	ENLDO	**LDO enable pin.** ENLDO is pulled up internally to high. Leave ENLDO open to enable the LDO. Drive it low to turn off the LDO.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{INv}= 19 V, V_{OUT} = 5 V, L = 1.5 µH/10 mΩ, Fs = 700 kHz, T_J = +25°C, unless otherwise noted.

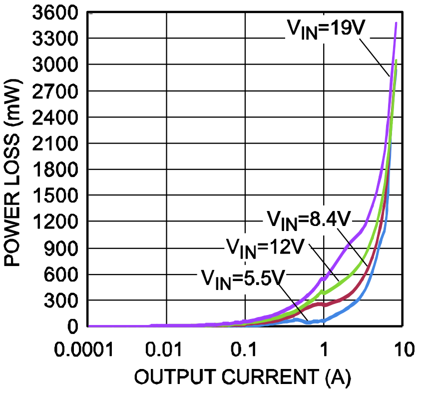
Efficiency vs. Load Current

V_{OUT}=5V,F_{SW}=700kHz,L=1.5µH, DCR=10mΩ,R_{BST}=3.3Ω,C_{OUT}=3x22uF



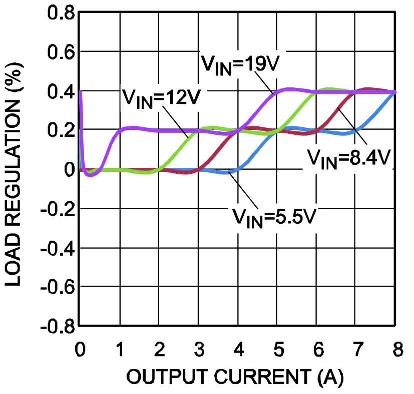
Power Loss

V_{OUT}=5V,F_{SW}=700kHz,L=1.5µH, DCR=10mΩ,R_{BST}=3.3Ω,C_{OUT}=3x22uF



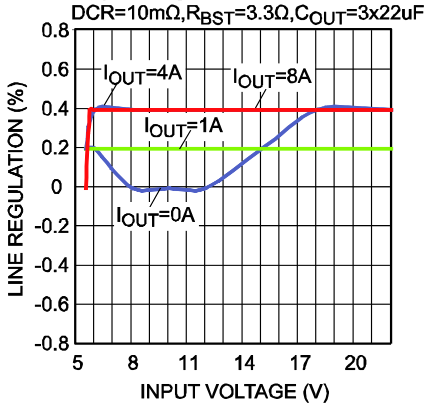
Load Regulation

V_{OUT}=5V,F_{SW}=700kHz,L=1.5µH, DCR=10mΩ,R_{BST}=3.3Ω,C_{OUT}=4x22uF

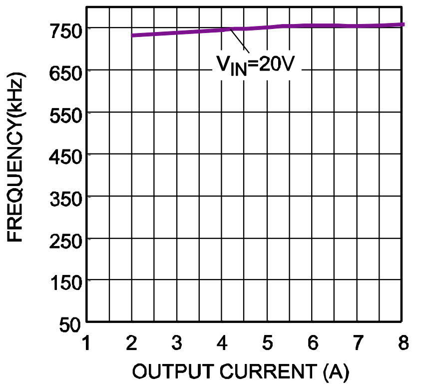


Line Regulation

V_{OUT}=5V,F_{SW}=700kHz,L=1.5µH, DCR=10mΩ,R_{BST}=3.3Ω,C_{OUT}=3x22uF

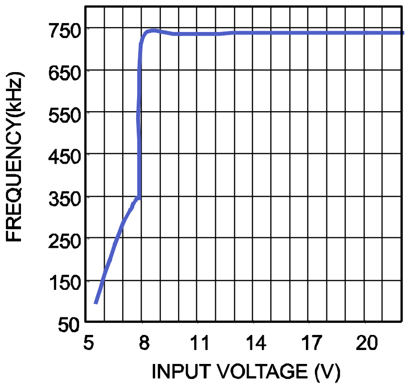


Switch Frequency vs. Output Current



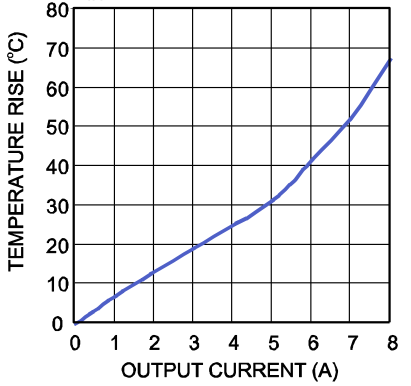
Switch Frequency vs. Output Current

I_{OUT}=2A



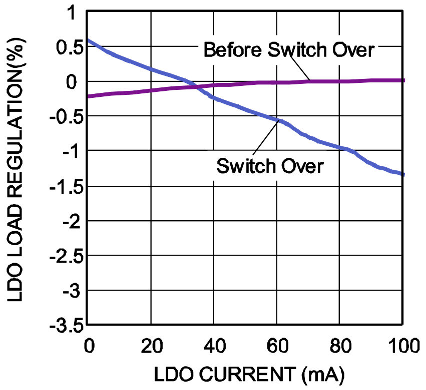
Temperature Rise vs. Load Current

V_{IN}=19V



LDO Load Regulation

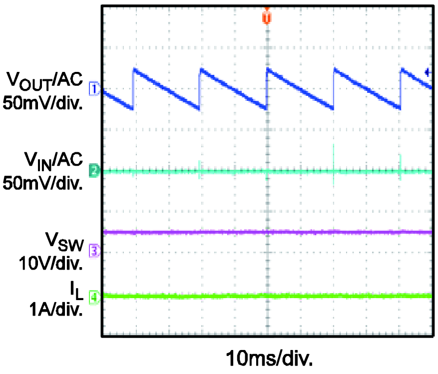
I_{OUT}=0.1A



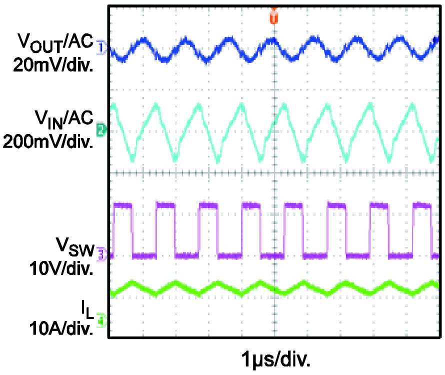
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19 V, V_{OUT} = 5 V, L = 1.5 µH/10 mΩ, Fs = 700 kHz, T_J=+25°C, unless otherwise noted.

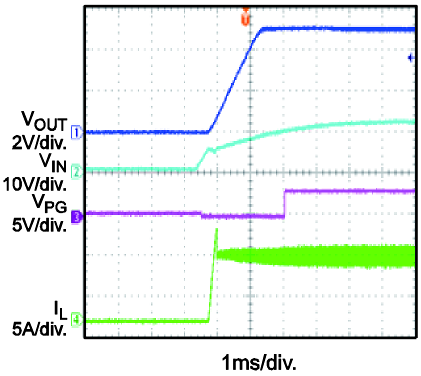
Input/Output Voltage Ripple
I_{OUT} = 0A



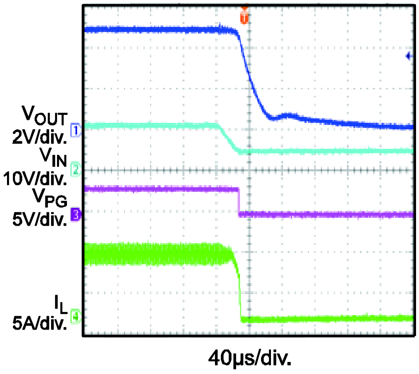
Input/Output Voltage Ripple
I_{OUT} = 8A



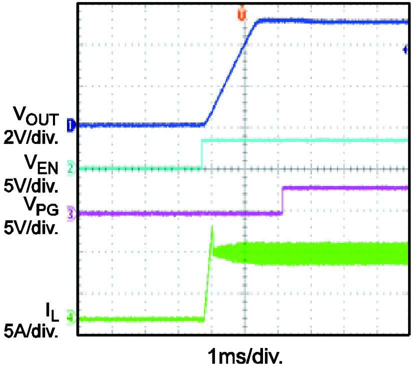
Power Good through V_{IN} Start-Up
I_{OUT} = 8A



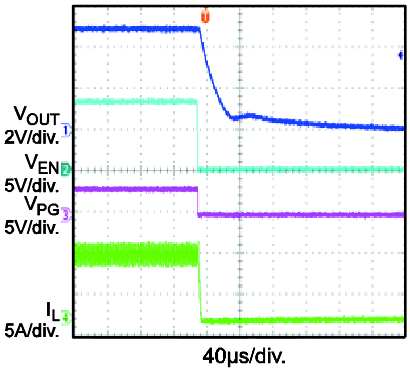
Power Good through V_{IN} Shutdown
I_{OUT} = 8A



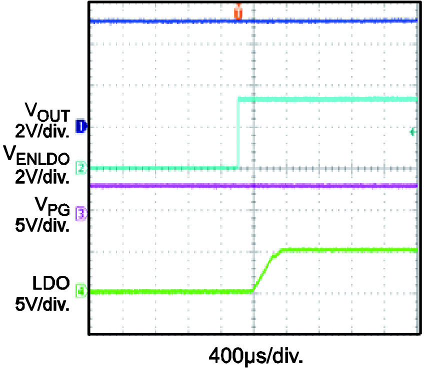
Power Good through EN Start-Up
I_{OUT} = 8A



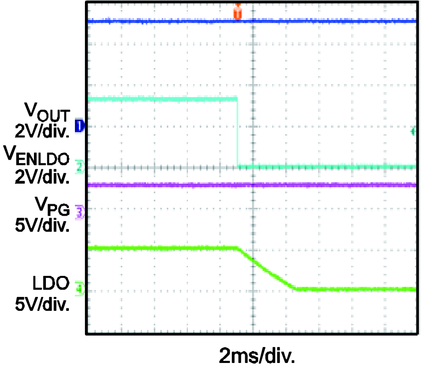
Power Good through EN Shutdown
I_{OUT} = 8A



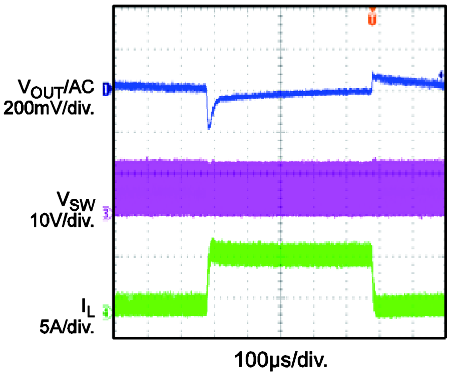
LDO Start Up through ENLDO
V_{IN} = 12V, I_{OUT} = 8A, I_{LDO} = 1mA



LDO Shutdown through ENLDO
V_{IN} = 12V, I_{OUT} = 8A, I_{LDO} = 1mA



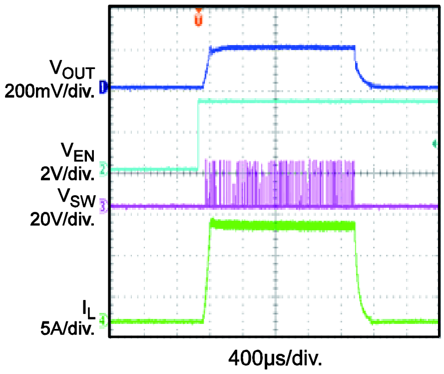
Transient
V_{IN} = 12V,L=1.5µH,C_{OUT}=88µF
I_{OUT}=1.2A-6.8A @1.6A/µs



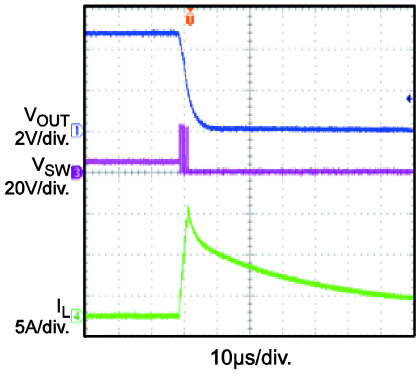
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}= 19 V, V_{OUT} = 5 V, L = 1.5 µH/10 mΩ, Fs = 700 kHz, T_J=+25°C, unless otherwise noted.

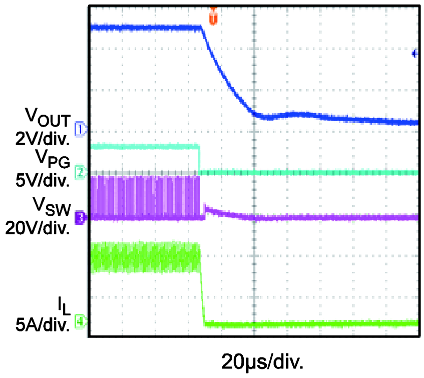
Short-Circuit Protection with EN On/Off
V_{IN} = 22V



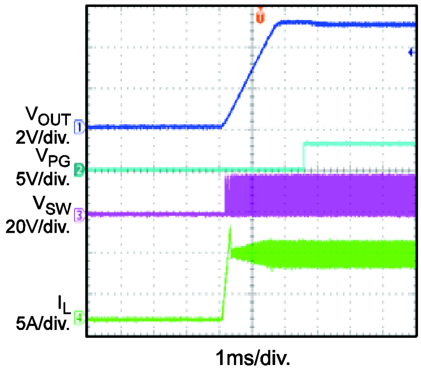
Short-Circuit Protection
V_{IN} = 22V



Thermal Shutdown
V_{IN} = 19V, I_{OUT} = 8A



Thermal Recovery
V_{IN} = 19V, I_{OUT} = 8A



FUNCTIONAL BLOCK DIAGRAM

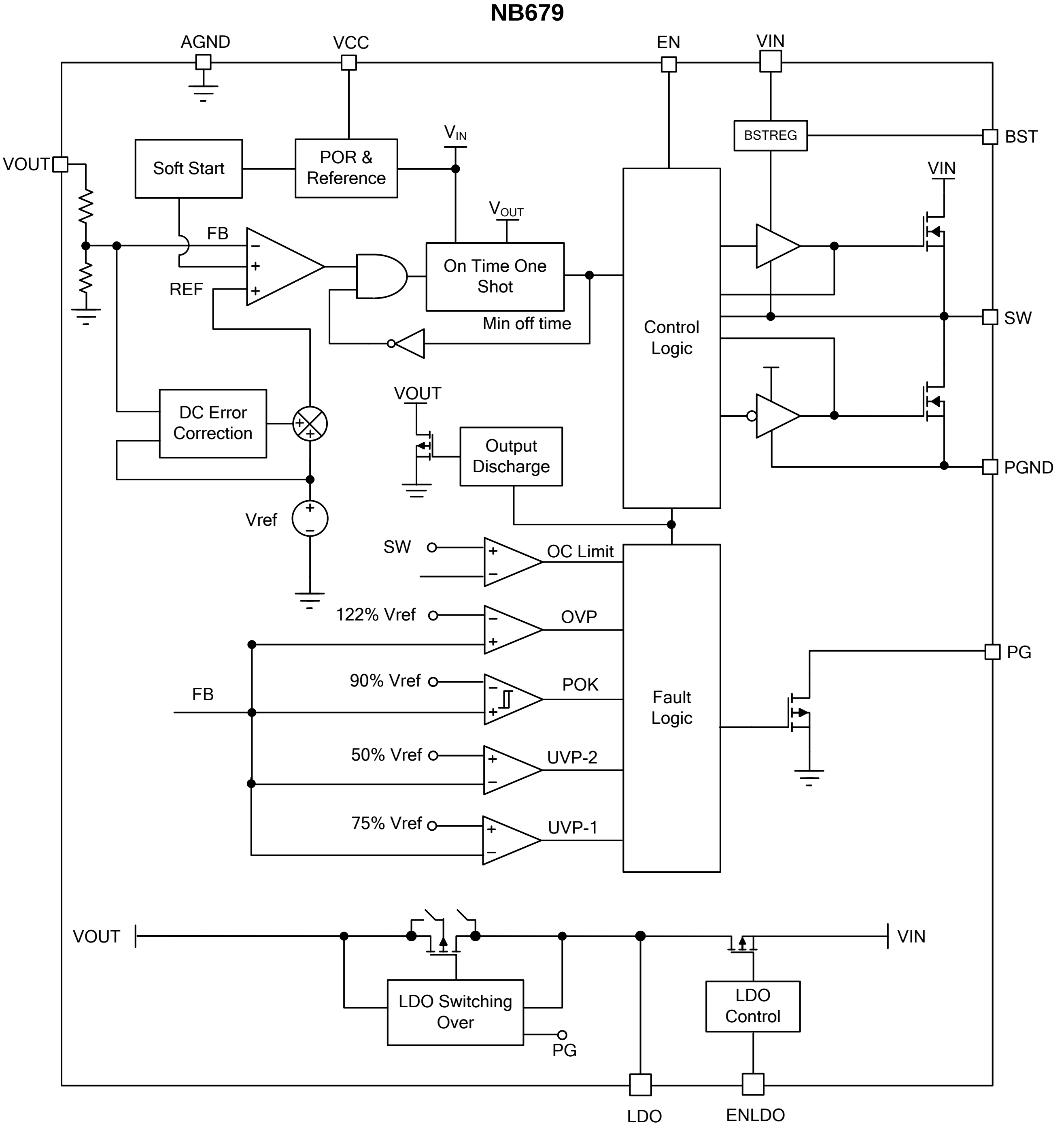


Figure 1—Functional block diagram of NB679

OPERATION

PWM Operation

The NB679 is a fully integrated, synchronous, rectified, step-down, switch-mode converter with a fixed 5 V output. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by the output voltage and the input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize the conduction loss. There is a dead short between the input and GND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

CCM Operation

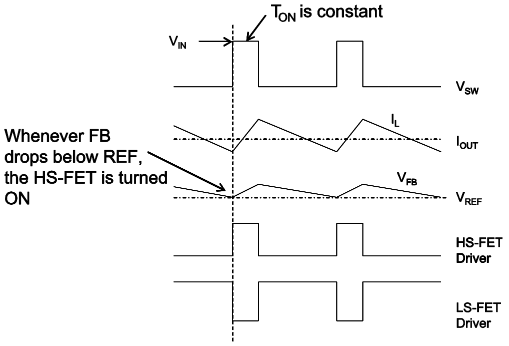


Figure 2—CCM operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (PWM mode).

DCM Operation

When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to discontinuous conduction mode (DCM).

DCM operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. See Equation (1). When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} does not reach V_{REF} when the inductor current approaches zero. The LS-FET driver turns into tri-state (high Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1 mA. Hence, the output capacitors discharge slowly to GND through the LS-FET. As a result, the efficiency at light-load is improved greatly. The HS-FET is not turned on as frequently during a light-load condition as it is during a heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the NB679 reduces the switching frequency naturally, achieving high efficiency at light load.

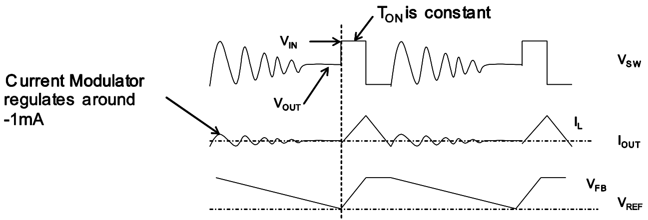


Figure 3—DCM operation

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

DC Auto-Tune Loop

NB679 applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF} by adjusting the comparator input REF to make V_{FB} always follow V_{REF}. The small DC loop improves the load and line regulation without affecting transient performance. The relationship between V_{FB}, V_{REF}, and REF is shown in Figure.4

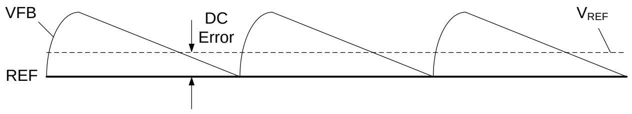


Figure 4—DC auto-tune loop operation

Large Duty Operation

The NB679 supports larger duty operation (5.5 V-5 V) by its internal Ton extension function. When the parts detects its FB is lower than Vref and Vin - Vo < 2 V, the Ton can be extended, extending the duty. If FB > REF or Ton reaches its limitation, Ton will stop extending.

Light load Ultrasonic Mode

Ultrasonic mode (USM) keeps the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects both the HS-FET and the LS-FET are off (for about 30 µs), it shrinks the Ton so as to keep Vout under regulation with optimal efficiency. If the load continues to reduce, the part discharges the Vout to make sure FB is smaller than 102 percent of the internal reference. The HS-FET turns on again once the internal FB reaches VREF and then stops switching.

USM is selected by the EN voltage level. When EN is in the range of 1.4 V to 1.8 V, it enters USM. If EN is in the range of 2.6 V to 3.6 V, it operates in normal mode.

Configuring the EN Control

The NB679 has two enable pins to control the on/off of the internal regulators and LDO.

For NB679, the buck regulator and LDO are controlled by EN and ENLDO, respectively. For example, when the application is only used with the buck regulator, the buck regulator is realized by pulling ENLDO low, allowing the buck to be controlled by EN.

See Table 2 for the NB679 EN logics.

Table 2—ENLDO/EN control

State	ENLDO	EN	VCC	VOUT	5V LDO
S0	1	1	ON	ON	ON
S3	1	0	ON	OFF	ON
S5	0	0	OFF	OFF	OFF
Others	0	1	ON	ON	OFF

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. Refer to the “UVLO Protection” section for more details.

Soft Start (SS)

The NB679 employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually; this causes the output voltage to ramp up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the part enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

5 V Linear Regulator

There is a built-in 100 mA standby linear regulator with a fixed output at 5 V, controlled by ENLDO. The 5 V LDO is intended mainly for an auxiliary 5 V supply for the notebook system during standby mode.

Add a ceramic capacitor with a value between 4.7 µF and 22 µF placed close to the LDO pins to stabilize the LDOs.

LDO Switch Over

When the output voltage becomes higher than 4.8 V (and the power good is ok), the internal LDO is switched over to VOUT by the internal MOSFET. This helps reduce the power loss from the LDO.

Power Good (PG)

The NB679 has power good (PG) output used to indicate whether the output voltage of the buck regulator is ready. PG is the open drain of a MOSFET. It should be connected to V_{CC} or another voltage source through a resistor (e.g. 100 k). After the input voltage is applied, the MOSFET is turned on so that PG is pulled to GND before SS is ready. After the FB voltage reaches 95 percent of the REF voltage, PG is pulled high after 750 µs. When the FB voltage drops to 85 percent of the REF voltage, PG is pulled low.

Over-Current Protection (OCP)

NB679 has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the HS-FET off and LS-FET on state, the OC trip level sets the valley level of the inductor current. Thus, the load current at the over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \tag{2}$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off. Eventually, it ends up crossing the under-voltage protection threshold and shuts down. Fault latching can be re-set by EN going low or the power cycling of VIN.

Over/Under-Voltage Protection (OVP/UVP)

NB679 monitors the output voltage to detect over and under voltage. Once the feedback voltage becomes higher than 122 percent of the target voltage, the OVP comparator output goes high, and the circuit latches as the HS-FET driver turns off, and the LS-FET driver turns on, acting as an -1.8 A current source.

When the feedback voltage drops below 75 percent of the Vref but remains higher than 50 percent, the UVP-1 comparator output goes high. The part is latched if the FB voltage remains in this range for about 32 µs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current hits zero. During this period, the valley current limit helps control the inductor current.

When the feedback voltage drops below 50 percent of the Vref, the UVP-2 comparator output goes high, and the part is latched off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current hits zero. Fault latching can be re-set by EN going low or the power cycling of VIN.

UVLO Protection

The part starts up only when the Vin voltage is higher than the UVLO rising threshold voltage. The part shuts down when VIN is lower than the Vin falling threshold. The UVLO protection is non-latch off. Fault latching can be re-set by EN going low or the power -cycling of VIN.

If an application requires a higher under-voltage lockout (UVLO), use EN (see Figure 5) to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the Vin falling threshold above 5.5 V. The rising threshold should be set to provide enough hysteresis to allow for any input supply variations.

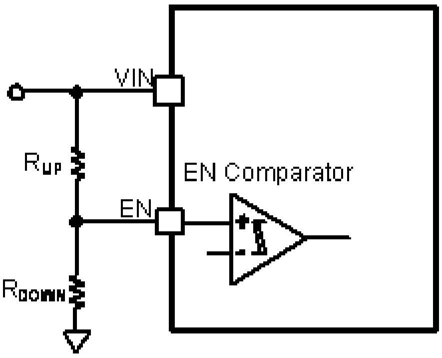


Figure 5—Adjustable UVLO

To avoid too much sink current on EN, the EN resistor (Rup) is usually in the range of 1 M-2 MΩ. A typical pull-up resistor is 2 MΩ.

Thermal Shutdown

Thermal shutdown is employed in the NB679. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (140ºC, typically), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 115ºC, it initiates a SS.

Output Discharge

NB679 discharges the output when EN is low, or the controller is turned off by the protection functions UVP, OCP, OCP, OVP, UVLO, and thermal shutdown. The part discharges outputs using an internal 6 Ω MOSFET.

APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple-current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3) and Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{3}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \tag{4}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated using Equation (5) and Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{5}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \tag{6}$$

Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \tag{7}$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{8}$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \tag{9}$$

The maximum output capacitor limitation should be considered in design application. For a small soft-start time period (if the output capacitor value is too high), the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately using Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \tag{10}$$

Where, I_{LIM_AVG} is the average start-up current during a soft-start period (it can be equivalent to the current limit value), and T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, resulting in a lower output ripple voltage. However, a larger value inductor has a larger physical footprint, a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 percent to 50 percent of the maximum output current, with the peak inductor current below the maximum switch current limit.

The inductance value can be calculated using Equation (11):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including short current), so it is suggested to choose Isat > 10 A.

PCB Layout Guidelines

Efficient PCB layout is critical for optimum IC performance. For best results, refer to Figure 6 and follow the guidelines below. For more information, refer to **AN087**.

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces. **The PGND trace should be as wide as possible (This should be the number one priority).**
2. Place the input capacitors as close to IN and GND as possible on the same layer as the IC.
3. Place the decoupling capacitor as close to VCC and GND as possible. Keep the switching node (SW) short and away from the feedback network.
4. Keep the BST voltage path as short as possible with >50 mil trace.
5. Keep the IN and GND pads connected with a large copper plane to achieve better thermal performance. Add several vias with 8 mil drill/16 mil copper width close to the IN and GND pads to help thermal dissipation.
6. A 4-layer layout is strongly recommended to achieve better thermal performance.

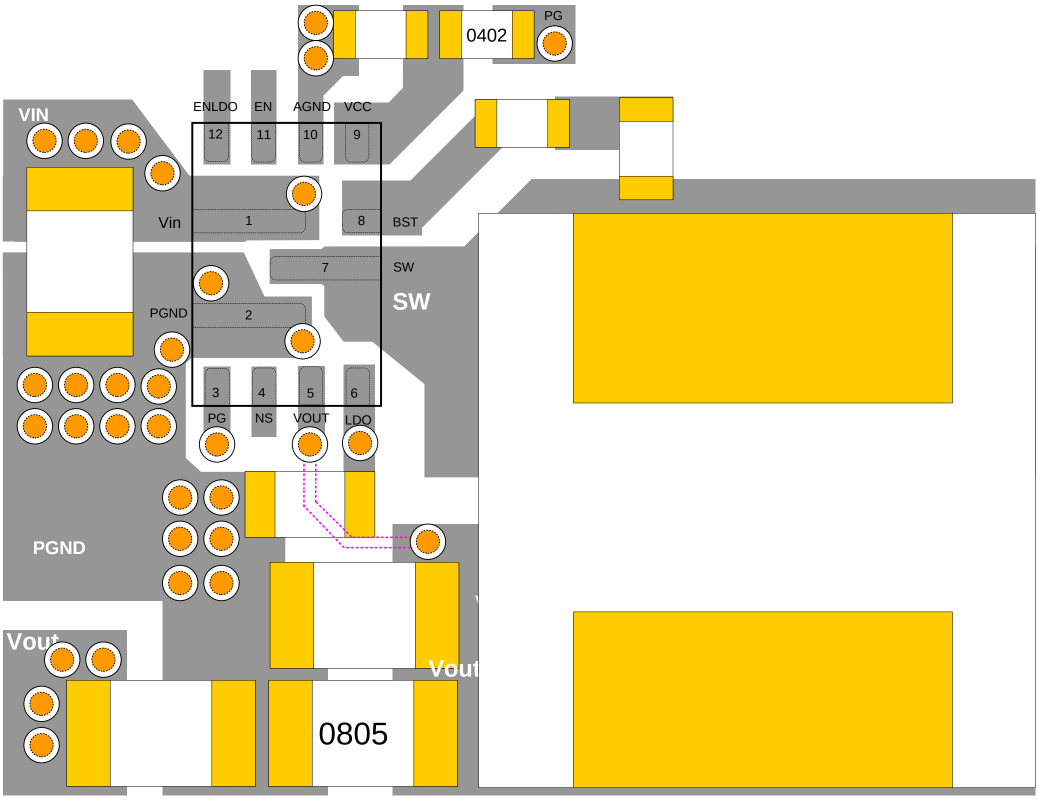


Figure 6—Recommended PCB layout

TYPICAL APPLICATION

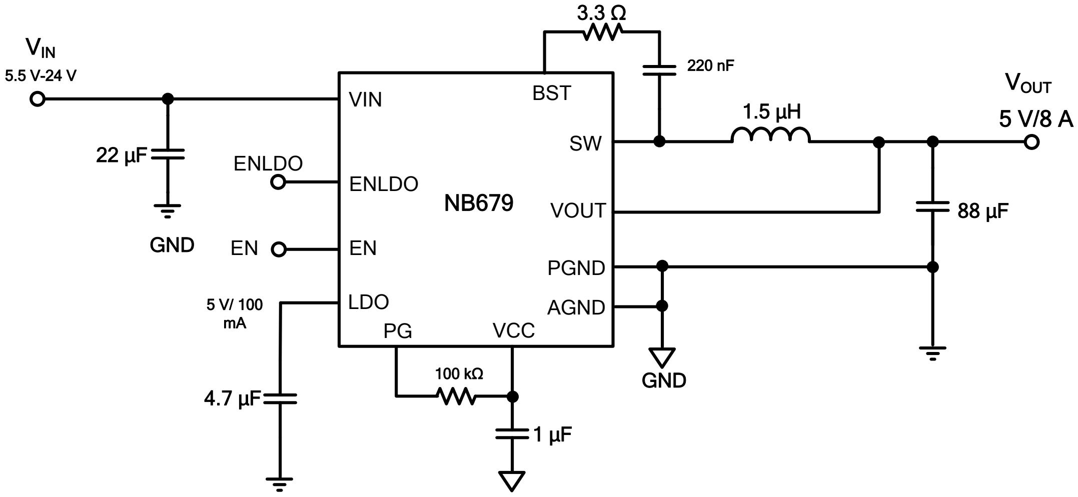


Figure 7— Typical application schematic with ceramic output capacitors

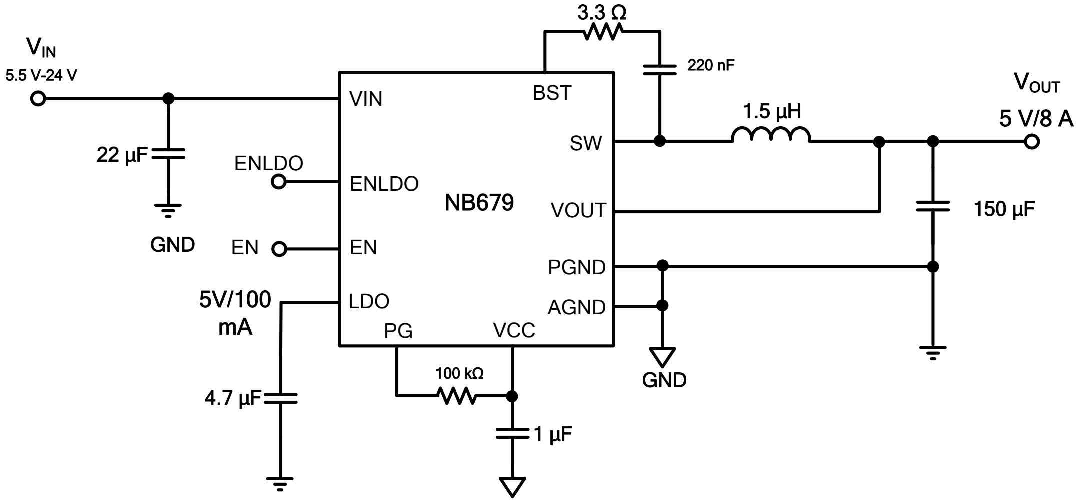
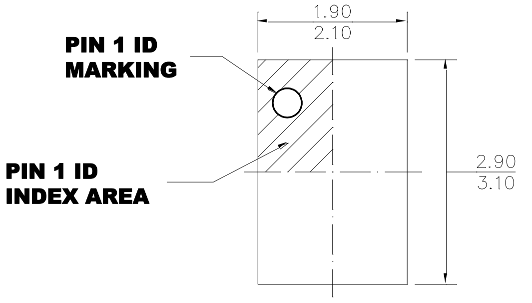


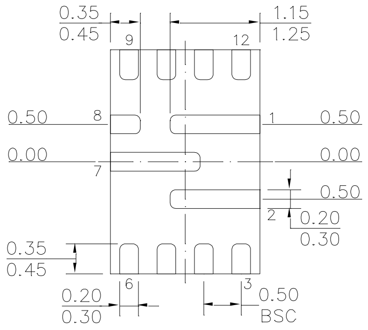
Figure 8— Typical application schematic with POSCAP output capacitors—recommended for large duty operation only.

PACKAGE INFORMATION

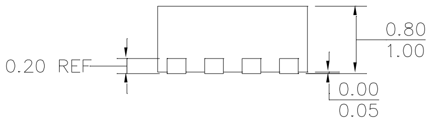
QFN-12 (2mm x 3mm)



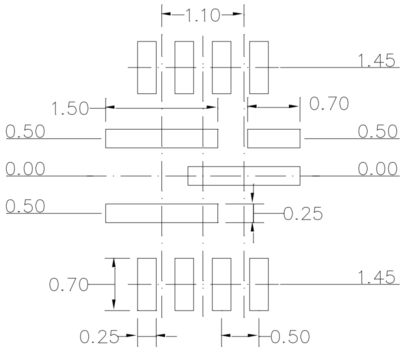
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.