

Ultra-Low On-Resistance, 6A Load Switch with Soft Start

Features

- **15mW(Typical) On-resistance**
- **6A Continuous Current**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Input Voltage Range (VIN): 0.8V to 5.5V**
- **Supply Voltage Range (VBIAS): 3V to 5.5V**
- **Output Discharge when Switch Disabled**
- **Reverse Current Blocking when Switch Disabled**
- **Over-Temperature Protection**
- **Enable Input**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

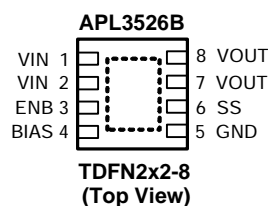
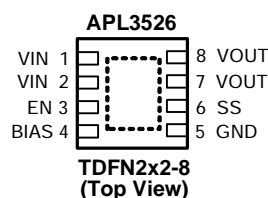
The APL3526/B is an ultra-low on-resistance, power-distribution switch with external soft start control. It integrates a N-channel MOSFET that can deliver 6A continuous load current each.

The device integrates over-temperature protection. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 160°C and will automatically turns on the power switch when the temperature drops by 40°C. The device is available in lead free TDFN2x2-8 packages.

Applications

- **Notebook**
- **AIO PC**

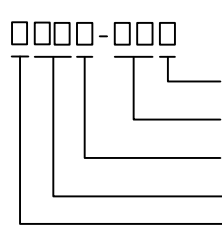
Pin Configurations



 = Exposed Pad (connected to ground plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APL3526 □□□□-□□□□</p>  <p> Assembly Material Handling Code Temperature Range Package Code Enable Function </p>	<p> Enable Function Blank : Active High B : Active Low Package Code QB : TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device </p>
<p>APL3526 QB: L26 • X X-Date Code</p>	
<p>APL3526B QB: 26B • X X-Date Code</p>	

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{BIAS}	BAIS to GND Voltage	-0.3 ~ 6	V
V_{IN}	VIN to GND Voltage	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 6	V
V_{EN}, V_{ENB}	EN or ENB to GND Voltage	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air <small>(Note 2)</small>	75	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN2x2-8 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{BIAS}	BIAS Input Voltage ($V_{BIAS} \geq V_{IN}$)	3.0 ~ 5.5	V
V_{IN}	VIN Input Voltage	0.8 ~ 5.5	V
I_{OUT}	VOUT Output Current	0 ~ 6	A
	Maximum Pulsed Switch Current, Pulse<300 μ s, 1% Duty Cycle	8	A
V_{EN}, V_{ENB}	Input Logic High	1.2 ~ 5.5	V
	Input Logic Low	0 ~ 0.4	V
T_A	Ambient Temperature	-40 ~ 85	$^{\circ}$ C
T_J	Junction Temperature	-40 ~ 125	$^{\circ}$ C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN} = 0.8V \sim 5V$, $V_{BIAS} = 5V$, $V_{EN} = \text{High}$ or $V_{ENB} = \text{Low}$, and $T_A = -40 \sim 85^{\circ}\text{C}$. Typical values are at $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Test Conditions	APL3526/B			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	BIAS Supply Current	No load	-	50	90	μ A
	BIAS Supply Current at Shutdown	No load, $V_{EN}=0V$	-	-	2	μ A
		No load, $V_{ENB}=5V$	-	-	10	μ A
	VIN Off-State Supply Current	No load, $V_{BIAS}=5V$, $V_{EN}=0V$ or $V_{ENB}=5V$, $V_{IN}=5V$	-	0.1	8	μ A
		No load, $V_{BIAS}=5V$, $V_{EN}=0V$ or $V_{ENB}=5V$, $V_{IN}=3.3V$	-	0.1	3	μ A
		No load, $V_{BIAS}=5V$, $V_{EN}=0V$ or $V_{ENB}=5V$, $V_{IN}=1.8V$	-	0.1	2	μ A
		No load, $V_{BIAS}=5V$, $V_{EN}=0V$ or $V_{ENB}=5V$, $V_{IN}=0.8V$	-	0.1	1	μ A
	Reverse Leakage Current	$V_{EN}=0V$ or $V_{ENB}=5V$, $V_{IN}=0V$	-	0.1	16	μ A
UNDER-VOLTAGE LOCKOUT (UVLO)						
	Rising BIAS UVLO Threshold	V_{BIAS} rising	1.9	2.4	2.9	V
	BIAS UVLO Hysteresis		-	0.1	-	V
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	$V_{BIAS}=5V$, $V_{IN}=0.8 \sim 5V$, $I_{OUT}=1A$, $T_J=25^{\circ}\text{C}$	-	15	20	m Ω
		$V_{BIAS}=5V$, $V_{IN}=0.8 \sim 5V$, $I_{OUT}=1A$, $T_J=-40 \sim 125^{\circ}\text{C}$	-	-	27	m Ω
		$V_{BIAS}=3.3V$, $V_{IN}=0.8 \sim 3.3V$, $I_{OUT}=1A$, $T_J=25^{\circ}\text{C}$	-	17	23	m Ω
		$V_{BIAS}=3.3V$, $V_{IN}=0.8 \sim 3.3V$, $I_{OUT}=1A$, $T_J=-40 \sim 125^{\circ}\text{C}$	-	-	31	m Ω
	VOUT Discharge Resistance	$V_{EN}=0V$ or $V_{ENB}=5V$, VOUT force 1V	-	100	150	Ω
SOFT-START CONTROL PIN						
	SS Discharge Current	$V_{SS}=6V$, $V_{EN}=0V$ or $V_{ENB}=5V$, measured at SS	-	560	-	μ A

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN} = 0.8V\sim 5V$, $V_{BIAS} = 5V$, $V_{EN} = \text{High}$ or $V_{ENB} = \text{Low}$, and $T_A = -40\sim 85^\circ C$. Typical values are at $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	APL3526/B			Unit
			Min.	Typ.	Max.	
EN OR ENB INPUT PIN						
V_{EN}, V_{ENB}	Input Logic High		1.2	-	-	V
	Input Logic Low		-	-	0.4	V
	Input Current		-	-	1	μA
OVERT-TEMPERATURE PROTECTION (OTP)						
	Over-Temperature Threshold	T_J rising	-	160	-	$^\circ C$
	Over-Temperature Threshold Hysteresis	T_J falling	-	40	-	$^\circ C$

Timing Chart

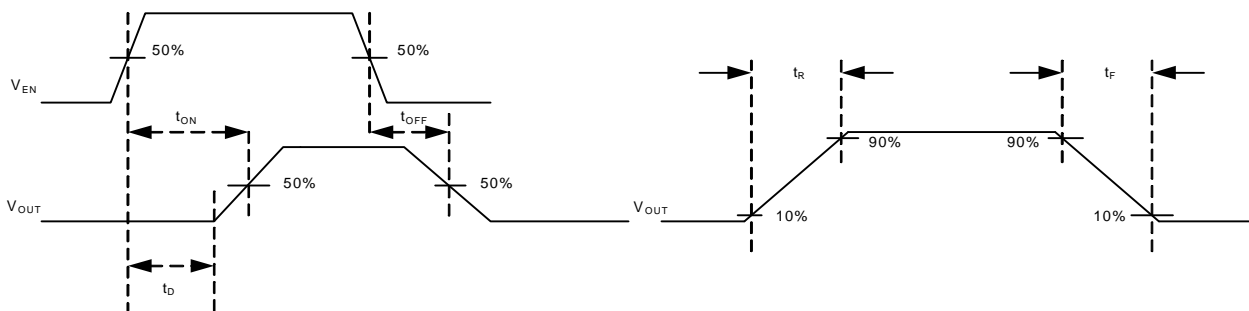
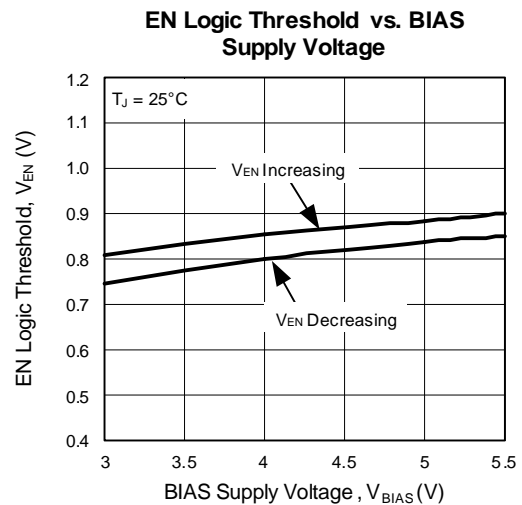
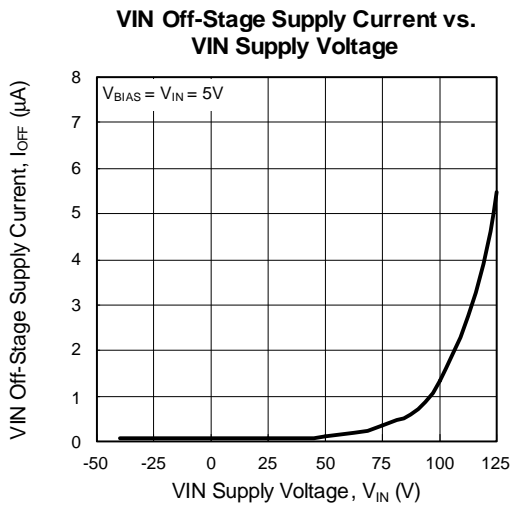
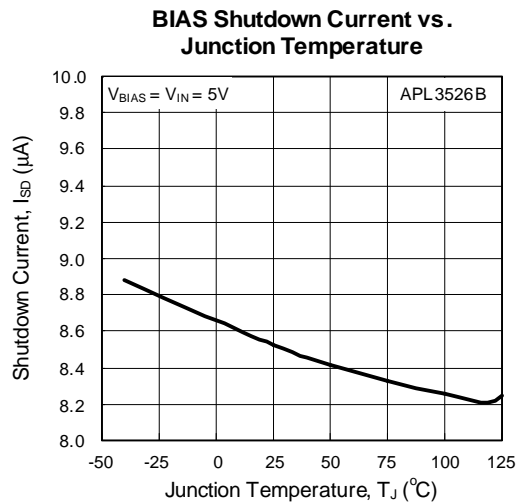
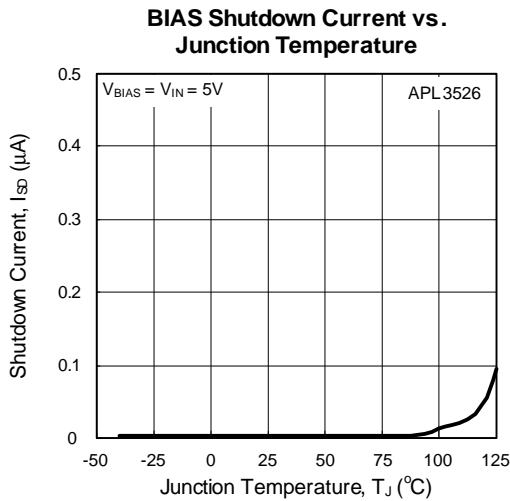
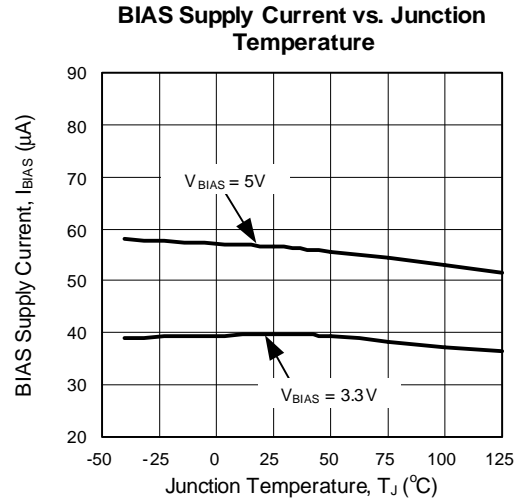
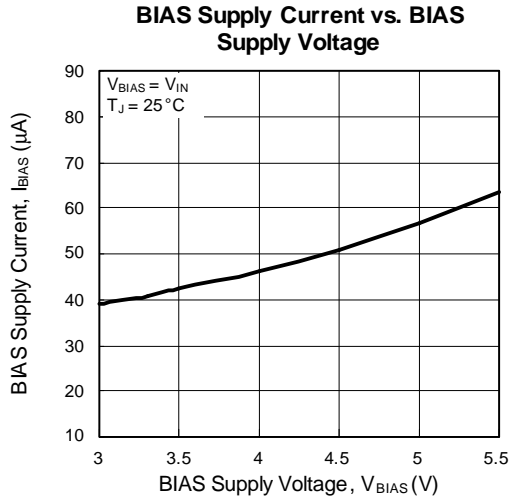


Figure 1. $t_{ON}/t_{OFF}, t_R/t_F$ Waveforms

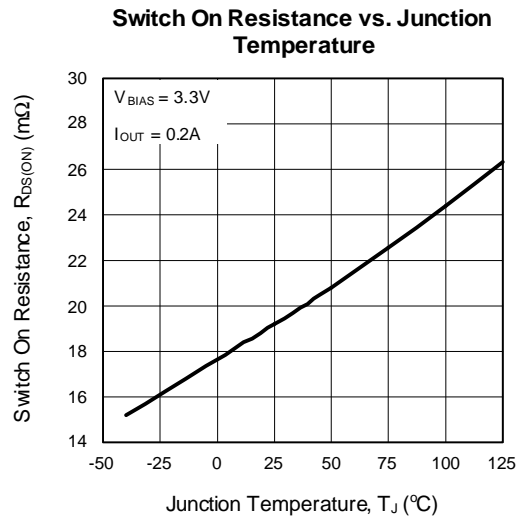
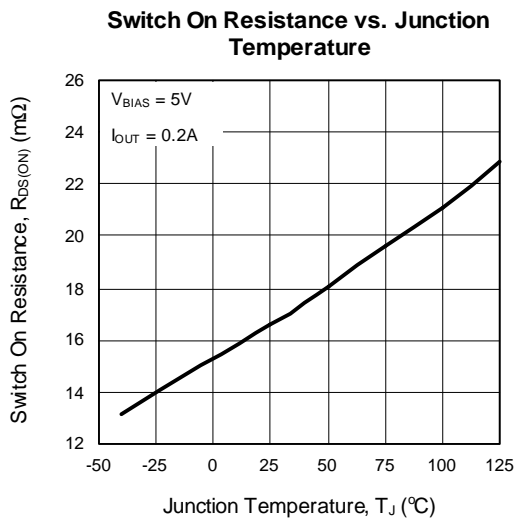
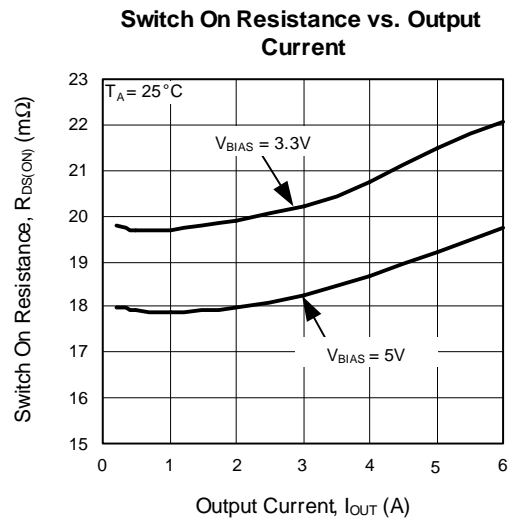
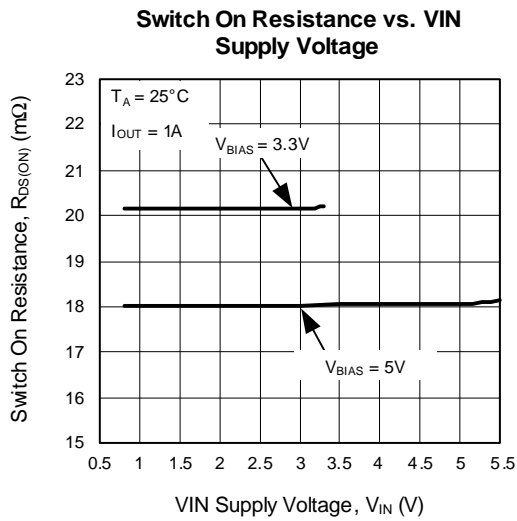
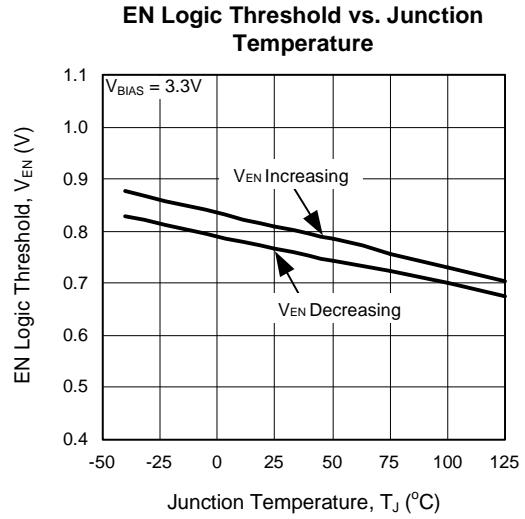
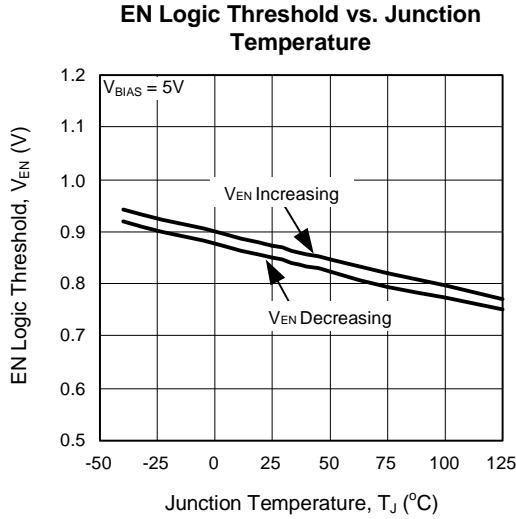
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Power supply Input of switch. Connect this pin to an external DC supply.
2	VIN	
3	EN	Enable input of switch. Logic high turns on switch. The EN pin cannot be left floating.
	ENB	Enable input of switch. Logic low turns on switch. The ENB pin cannot be left floating.
4	BIAS	Bias voltage input pin for internal control circuitry.
5	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
6	SS	Soft start control of switch. A capacitor from this pin to ground sets the VOUT's rise slew rate.
7	VOUT	Switch output.
8	VOUT	
Exposed Pad		Connect this pad to system ground plane for good thermal conductivity.

Typical Operating Characteristics

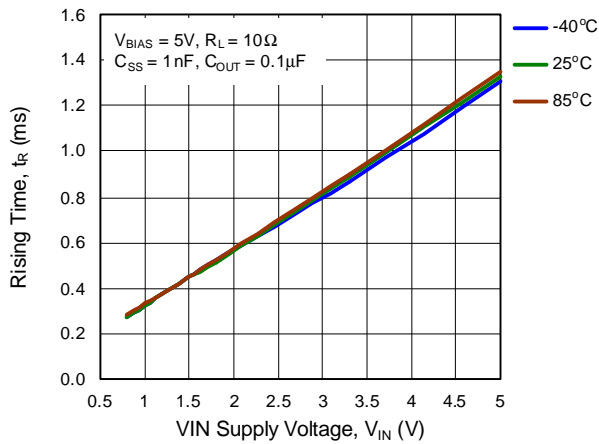


Typical Operating Characteristics

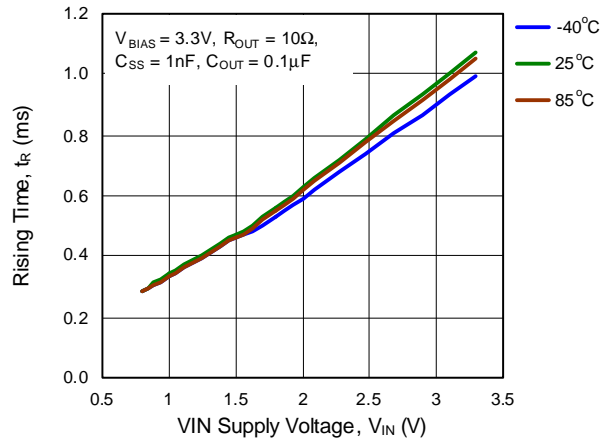


Typical Operating Characteristics

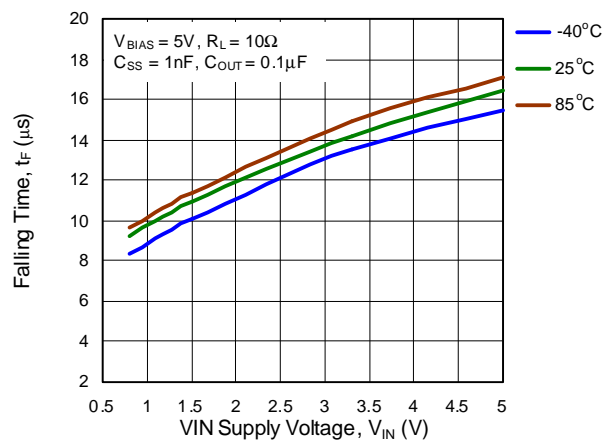
Rising Time vs. VIN Supply Voltage



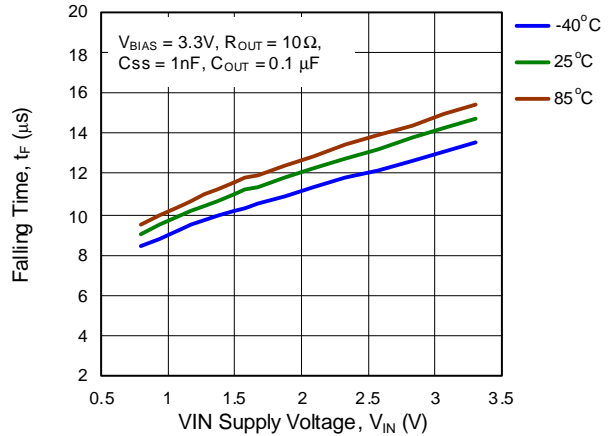
Rising Time vs. VIN Supply Voltage



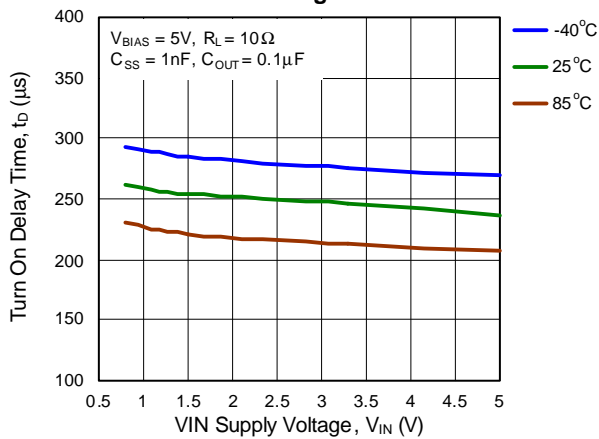
Falling Time vs. VIN Supply Voltage



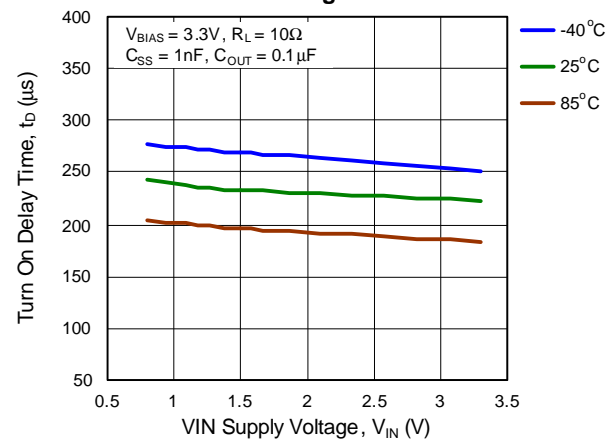
Falling Time vs. VIN Supply Voltage



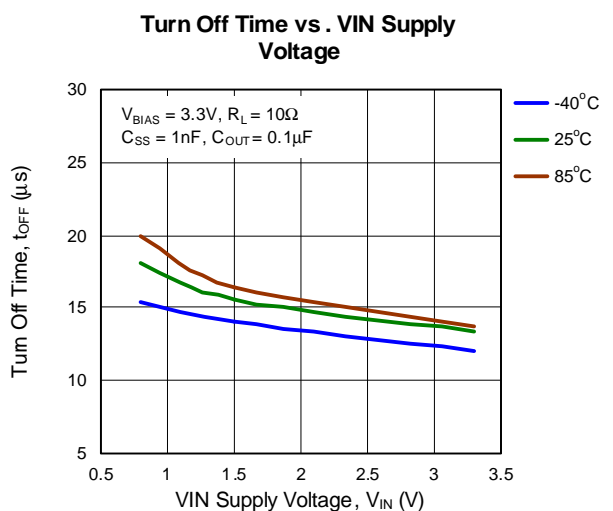
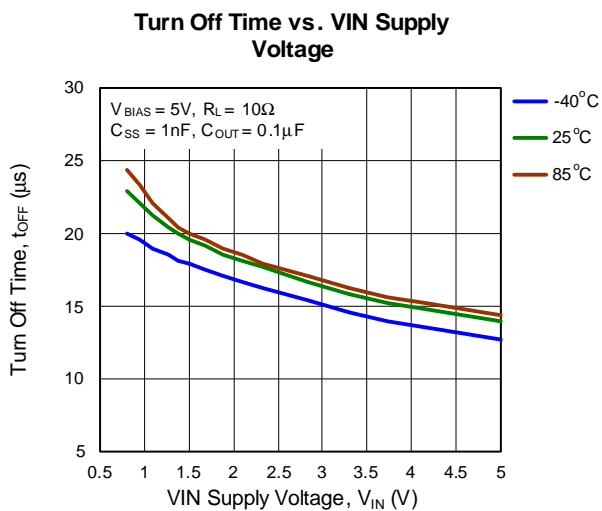
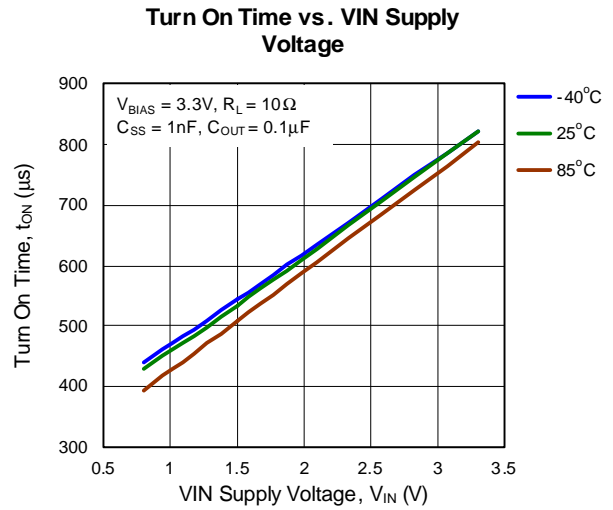
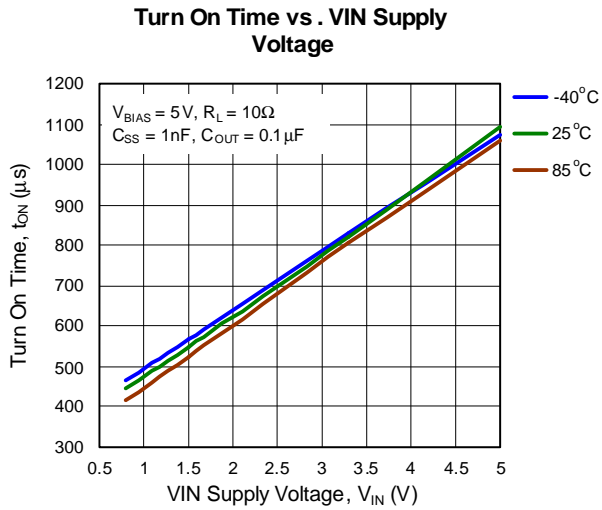
Turn On Delay Time vs. VIN Supply Voltage



Turn On Delay Time vs. VIN Supply Voltage

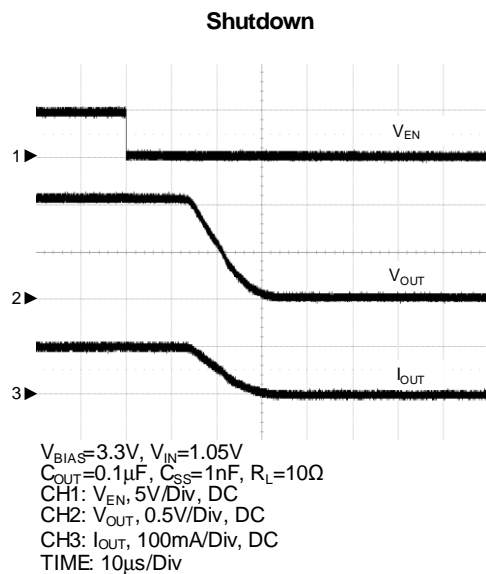
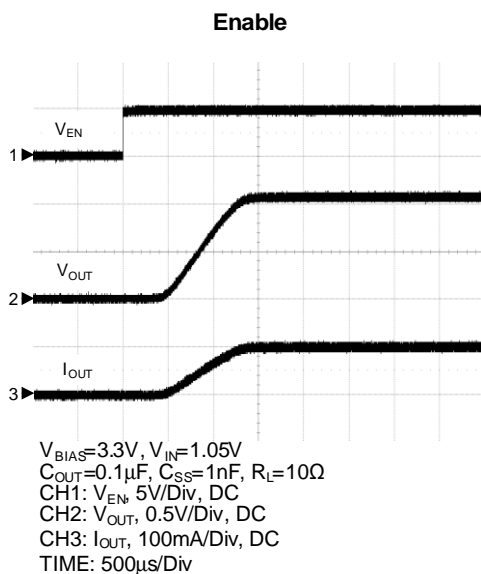
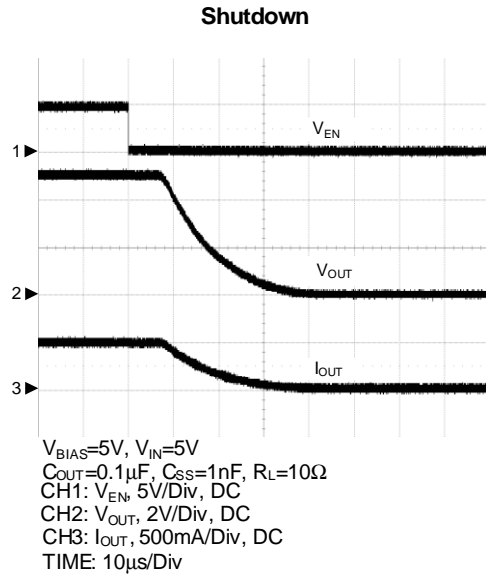
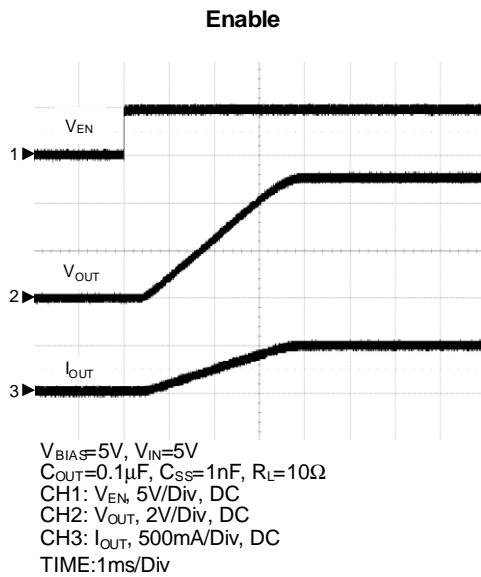


Typical Operating Characteristics

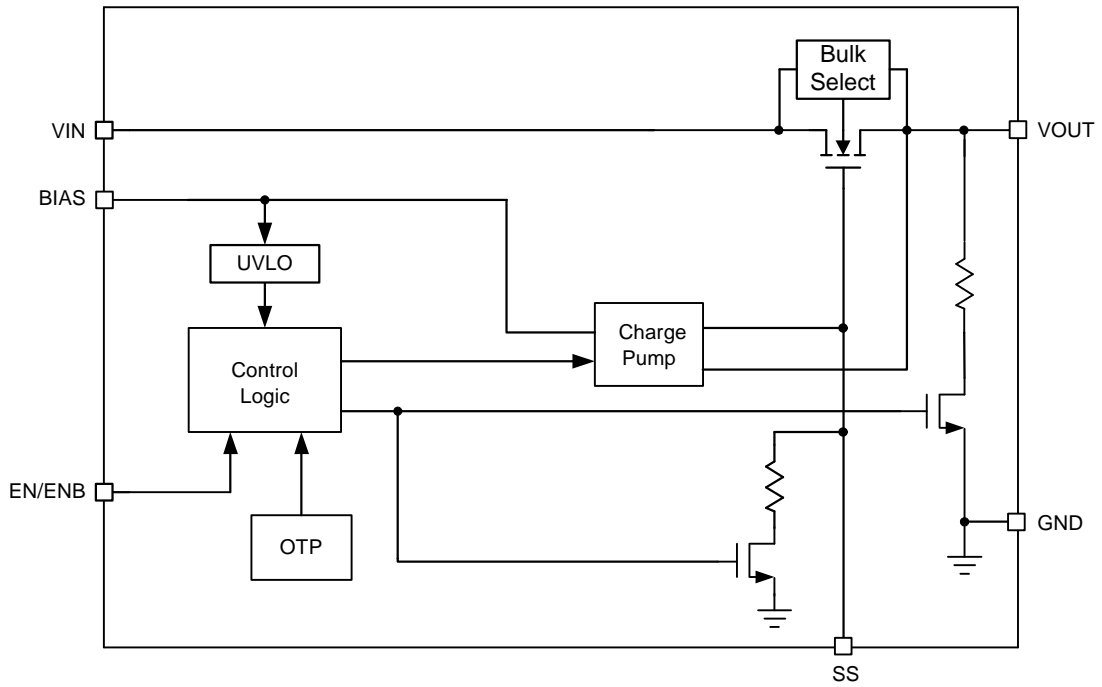


Operating Waveforms

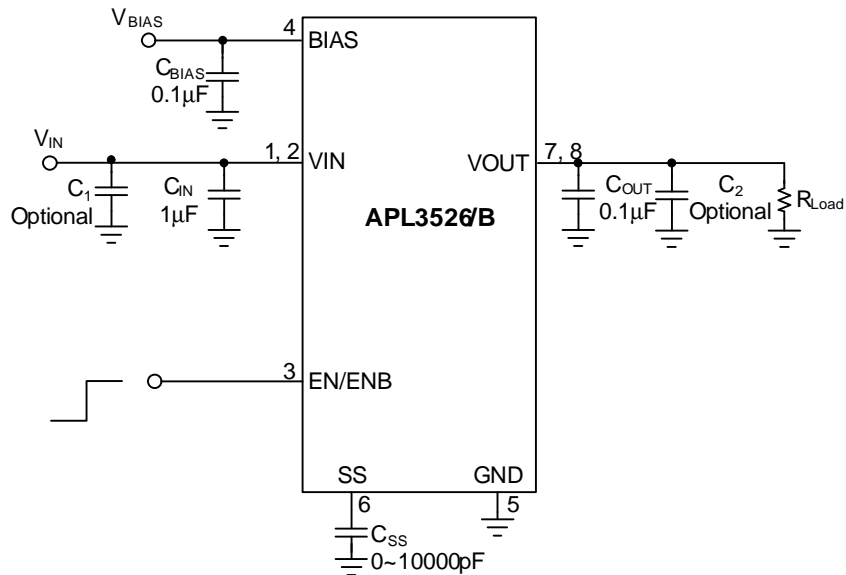
Refer to the typical application circuit. $T_A = 25^\circ\text{C}$ unless otherwise specified.



Block Diagram



Typical Application Circuit



Soft-Start Time

C _{SS} (pF)	Soft-Start Time (µs) 10% to 90%, V _{BIAS} =5V, C _L =0.1µF, C _{IN} =1µF, R _L =10Ω, Typical values are at T _A =25°C.						
	V _{IN} =5V	V _{IN} =3.3V	V _{IN} =1.8V	V _{IN} =1.5V	V _{IN} =1.2V	V _{IN} =1.05V	V _{IN} =0.8V
0	123	97	77	71	65	63	56
220	414	290	190	169	145	133	115
330	539	374	237	209	180	165	138
470	752	515	318	276	233	213	178
1000	1519	1016	605	523	441	398	330
2200	3047	2030	1186	1022	848	764	628
4700	6728	4425	2565	2196	1824	1626	1338
10000	14040	9183	5281	4531	3729	3334	2724

Soft-Start Time

C _{SS} (pF)	Soft-Start Time (μs) 10% to 90%, V _{BIAS} =3.3V, C _L =0.1μF, C _{IN} =1μF, R _L =10Ω, Typical values are at T _A =25°C.						
	-	V _{IN} =3.3V	V _{IN} =1.8V	V _{IN} =1.5V	V _{IN} =1.2V	V _{IN} =1.05V	V _{IN} =0.8V
0	-	115	82	74	67	64	58
220	-	336	201	174	148	138	117
330	-	429	252	216	184	168	143
470	-	595	333	286	240	218	183
1000	-	1185	645	542	452	408	338
2200	-	2367	1257	1050	872	781	643
4700	-	5140	2708	2269	1873	1664	1371
10000	-	10620	5560	4621	3795	3437	2764

Note 5: The table Contains soft-start time values measured on a typical device. The soft-start times shown are only valid for the powerup sequence where V_{IN} and V_{BIAS} are already in steady state condition, and EN pin is asserted high.

Function Description

BIAS Under-voltage Lockout (UVLO)

A under-voltage lockout (UVLO) circuit monitors the BIAS pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the BIAS supply voltages exceed rising UVLO voltage threshold during powering on.

Power Switch

The power switch is an N-channel MOSFET with a ultra-low $R_{DS(ON)}$. When IC is in shutdown state ($V_{EN}=Low$ or $V_{ENB}=High$), the MOSFET prevents a reverse current flowing from the VOUT back to VIN. When IC is in UVLO state, the internal parasitic diodes connected from VOUT to VIN will be forward biased.

Soft-start

The APL3526/B Provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground.

Enable Control

Pulling the ENB above 1.2V or EN below 0.4V will disable the device, and pulling ENB pin below 0.4V or EN above 1.2V will enable the device. The EN/ENB pins cannot be left floating.

Over-Temperature Protection (OTP)

When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed $T_j=+125^{\circ}C$.

Application Information

Power Sequencing

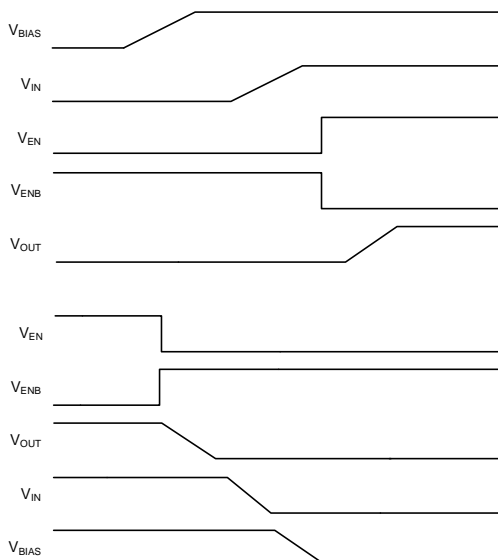


Figure 1. APL3526/B Power Sequencing Diagram

The APL3526/B has a built-in reverse current blocking circuit to prevent a reverse current flowing through the body diode of power switch from the VOUT back VIN pin when power switch disabled. The reverse current blocking circuit is not active before V_{BIAS} is ready. When IC is in UVLO state, the internal parasitic diodes of power switch connected from VOUT to VIN will be forward biased. Otherwise, VOUT should not be higher than VBIAS, and VBIAS must be higher than the voltage of any other input pin, the reason is that the internal parasitic diodes connected from VOUT to VBIAS will be forward biased.

Capacitor Selection

The APL3526/B requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

For normal applications (except OTP or output short circuit has occurred), the recommended input capacitance of VIN is 1 μ F. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during load transient conditions.

The recommended output capacitance of VOUT is 0.1 μ F at least. Please place the capacitors near the APL3526/B as close as possible.

A bulk output capacitor, placed close to the load, is recommended to support load transient current.

Soft-Start Capacitor

The soft-start capacitor on SS pin can reduce the inrush current and overshoot of output voltage. The soft-start time is set with a capacitor from the SS pin to the ground.

Thermal Consideration

The APL3526/B maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where $(T_J - T_A)$ is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the $T_A = 25^\circ\text{C}$ and maximum $T_J = 160^\circ\text{C}$ (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$\begin{aligned} P_{D(\max)} &= (160 - 25) / 75 \\ &= 1.8(\text{W}) \end{aligned}$$

For normal operation, do not exceed the maximum operating junction temperature of $T_J = 125^\circ\text{C}$. The calculated power dissipation should be less than:

$$\begin{aligned} P_D &= (125 - 25) / 75 \\ &= 1.33(\text{W}) \end{aligned}$$

$$\begin{aligned} P_D &= (125 - 85) / 75 \\ &= 0.53(\text{W}) \end{aligned}$$

The power dissipation depends on operating ambient temperature for fixed $T_J = 125^\circ\text{C}$ and thermal resistance θ_{JA} . For APL3526/B packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

Application Information

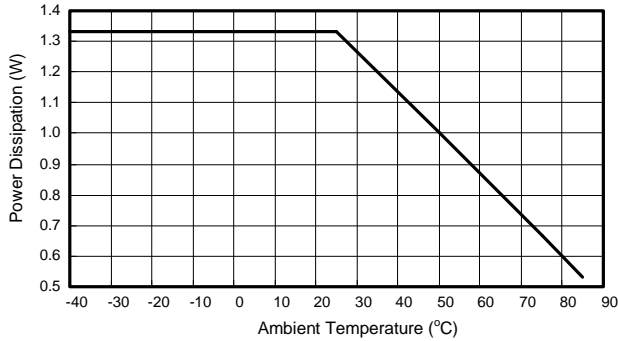


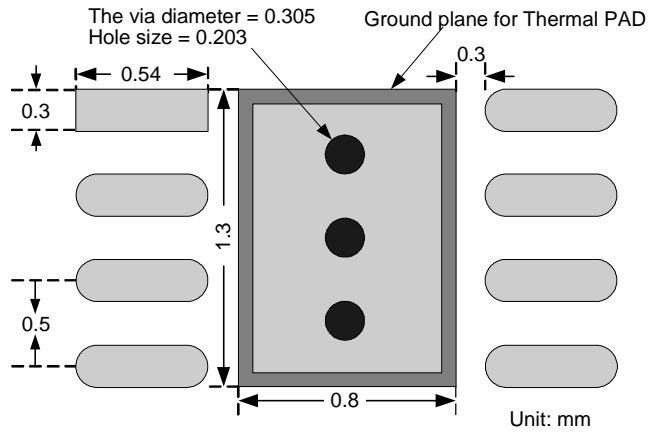
Figure 2. Derating Curves for APL3526/B Package

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3526/B and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep VIN and VOUT traces as wide and short as possible.

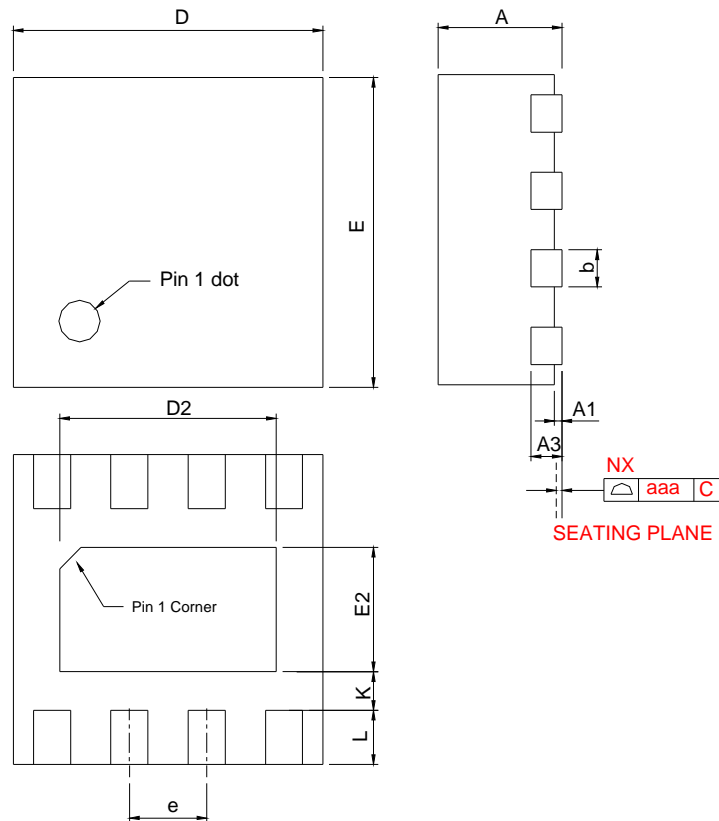
Recommended Minimum Footprint



TDFN2x2-8

Package Information

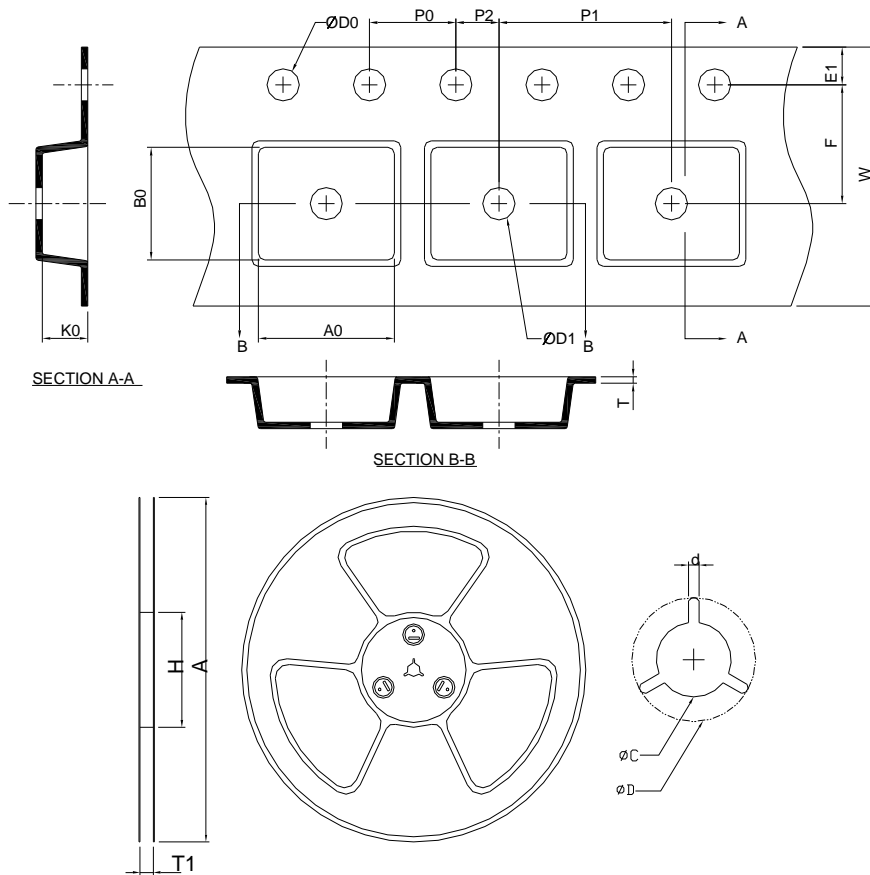
TDFN2x2-8



SYMBOL	TDFN2x2-8					
	MILLIMETERS			INCHES		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.03	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.24	0.30	0.007	0.010	0.012
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.00	1.30	1.60	0.039	0.051	0.063
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.60	0.80	1.00	0.024	0.032	0.039
e	0.50 BSC			0.020 BSC		
L	0.30	0.38	0.45	0.012	0.015	0.018
K	0.20			0.008		
aaa	0.08			0.003		

Note : 1. Follow from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	2.35±0.20	2.35±0.20	1.00±0.20

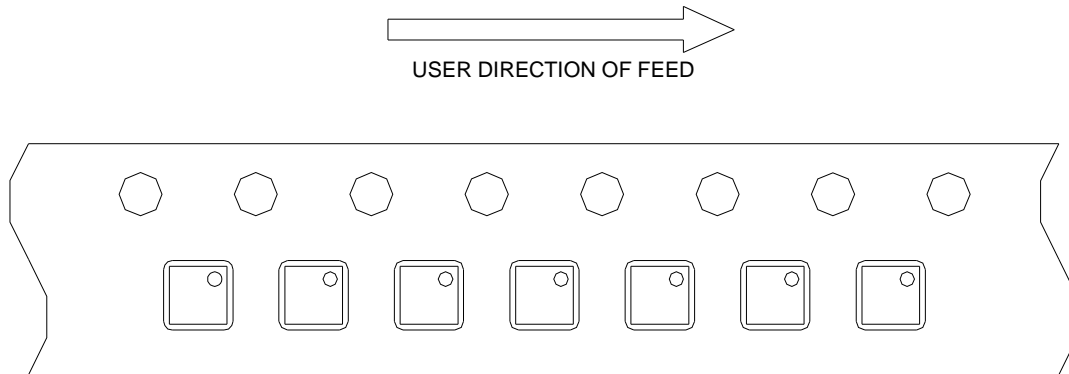
(mm)

Devices Per Unit

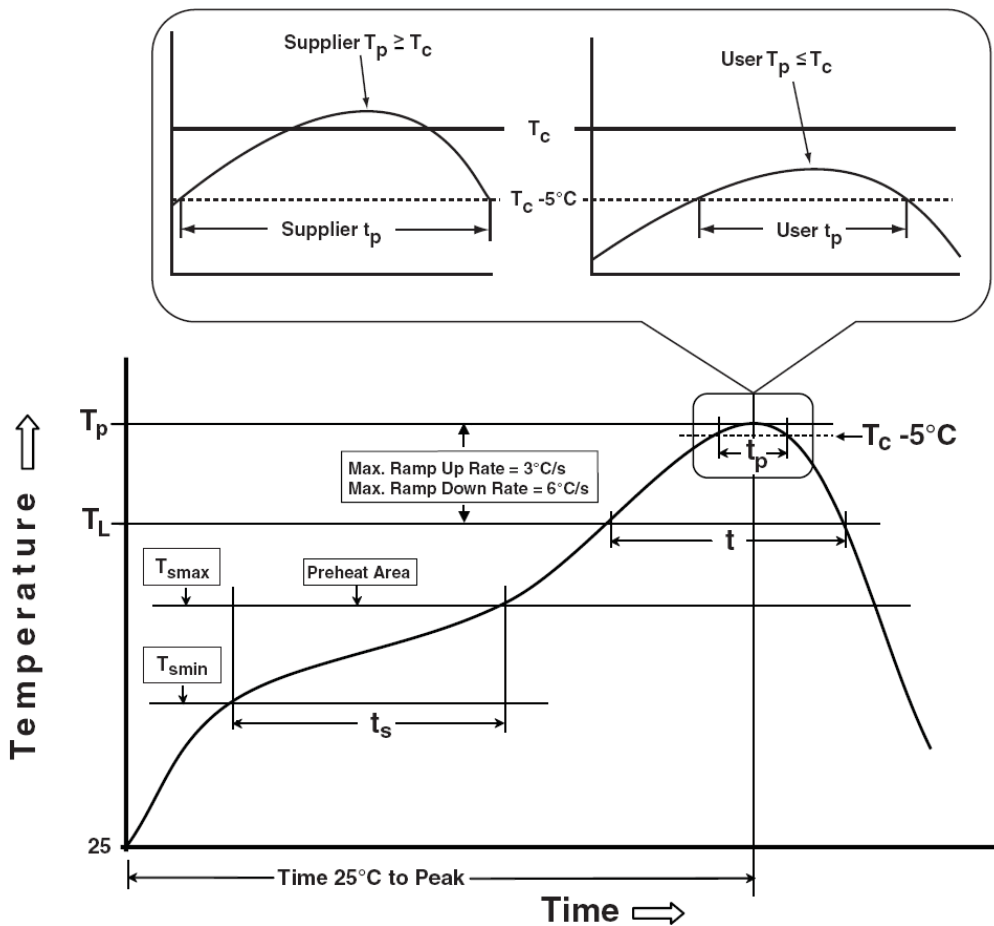
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $I_{tr} \geq 100\text{mA}$

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