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# STGAP2SICDTR

STMicroelectronics

Gate Drivers Galvanically isolated 4 A dual gate driver

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## Galvanically isolated 4 A dual gate driver



### Features

- High voltage rail up to 1200 V
- Driver current capability: 4 A sink/source @ 25 °C
- dV/dt transient immunity  $\pm 100$  V/ns
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- 4 A Miller CLAMP
- UVLO function
- Configurable interlocking function
- Dedicated SD and BRAKE pins
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function
- 6 kV galvanic isolation
- Wide Body SO-36W

### Application

- Motor driver for industrial drives, factory automation, home appliances and fans
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

### Description

The **STGAP2SiCD** is a dual gate driver for SiC MOSFETs which provides galvanic isolation between each gate driving channel and the low voltage control and interface circuitry. The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making it suitable for mid and high power applications such as power conversion and industrial motor drivers inverters. The separated output pins allow to independently optimize turn-on and turn-off by using dedicated gate resistors, while the Miller CLAMP function allows avoiding gate spikes during fast commutations in half-bridge topologies. The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems. In half-bridge topologies the interlocking function prevents outputs from being high at the same time, avoiding shoot-through conditions in case of wrong logic input commands. The interlocking function can be disabled by a dedicated configuration pin, allowing independent and parallel operation of the two channels. The input to output propagation delay results are contained within 75 ns, providing high PWM control accuracy. A standby mode is available in order to reduce idle power consumption.

#### Product status link

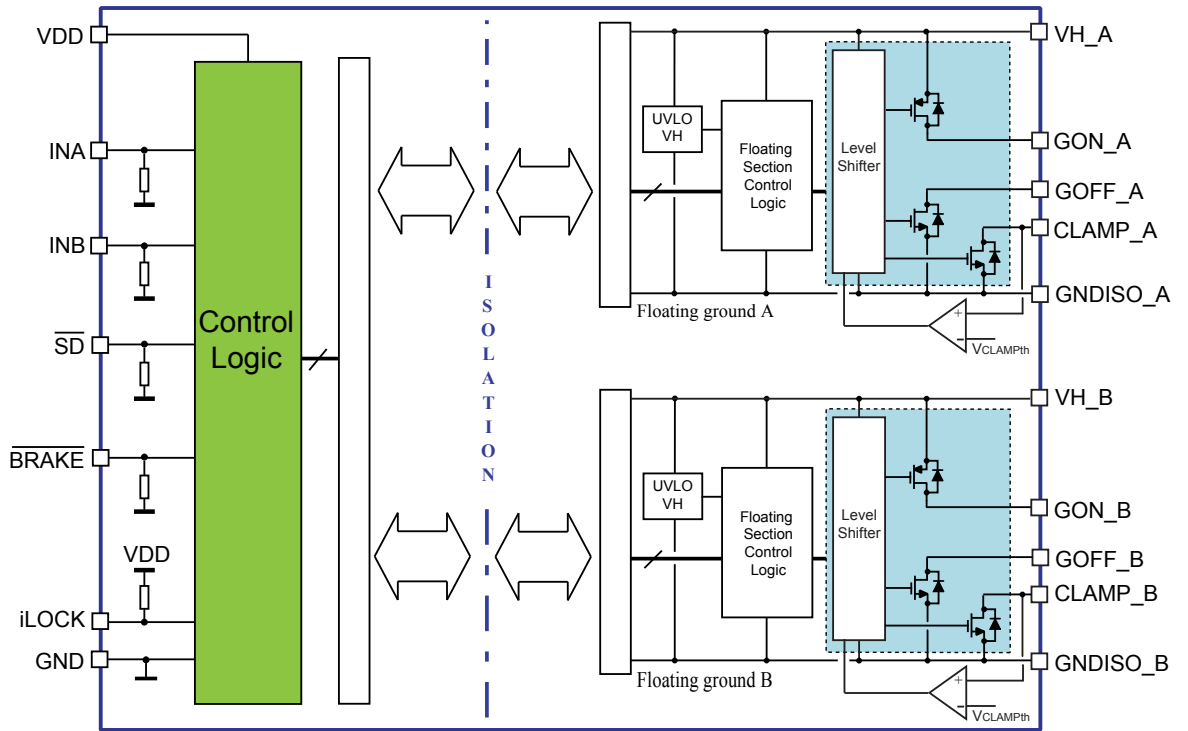
[STGAP2SiCD](#)

#### Product label



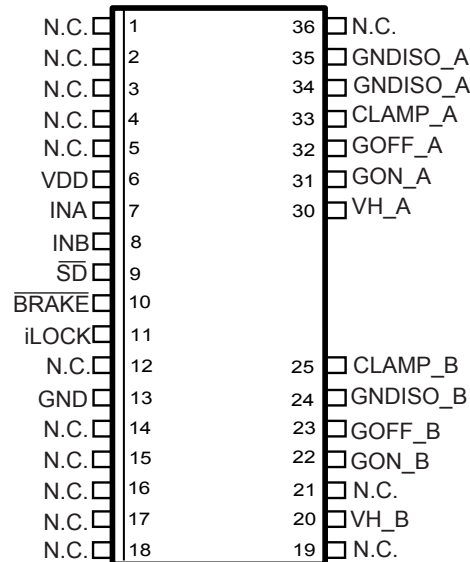
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description and connection diagram

**Figure 2. Pin connection (top view)**



**Table 1. Pin description**

Pin number	Pin name	Type	Function
6	VDD	Power supply	Control logic supply voltage
7	INA	Logic input	Control logic input for Channel A, active high
8	INB	Logic input	Control logic input for Channel B, active high
9	$\overline{SD}$	Logic input	Shutdown input, active low
10	$\overline{BRAKE}$	Logic input	Control logic input, active low
11	iLOCK	Analog input	Interlocking enable/disable
13	GND	Power supply	Control logic ground
20	VH_B	Power supply	Channel B gate driving positive supply
22	GON_B	Analog output	Channel B Source output
25	CLAMP_B	Analog output	Channel B Miller Clamp
23	GOFF_B	Analog output	Channel B Sink output
24	GNDISO_B	Power supply	Channel B gate driving isolated ground
30	VH_A	Power supply	Channel A gate driving positive supply
31	GON_A	Analog output	Channel A Source output
33	CLAMP_A	Analog output	Channel A Miller Clamp
32	GOFF_A	Analog output	Channel A Sink output
34, 35	GNDISO_A <sup>(1)</sup>	Power supply	Channel A gate driving isolated ground
1, 2, 3, 4, 5, 12, 14, 15, 16, 17, 18	N.C.	Not connected.	

1. Both GNDISO\_A pins must be connected and shorted together.

### 3 Electrical data

#### 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		-0.3	6.5	V
V <sub>LOGIC</sub>	Logic pins voltage vs. GND		-0.3	6.5	V
iLOCK	Interlocking Enable vs. GND		-0.3	VDD + 0.3	V
VH <sub>x</sub>	Positive supply voltage (VH <sub>x</sub> vs GNDISO <sub>x</sub> )		-0.3	28	V
V <sub>OUT</sub>	Voltage on gate driver outputs (GON <sub>x</sub> , GOFF <sub>x</sub> , CLAMP <sub>x</sub> vs GNDISO <sub>x</sub> )		-0.3	VH <sub>x</sub> + 0.3	V
T <sub>J</sub>	Junction temperature		-40	150	°C
T <sub>S</sub>	Storage temperature		-50	150	°C
ESD	HBM (human body model)			2	kV

#### 3.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Package	Value	Unit
R <sub>th(JA)</sub>	Thermal resistance junction to ambient	SO-36W	52	°C/W

### 3.3 Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		3.1	5.5	V
VLOGIC	Logic pins voltage vs. GND		0	5.5	V
iLOCK	Interlocking Enable vs. GND		0	VDD	V
VH_x	Positive supply voltage (VH_x vs. GNDISO_x)			26	V
GNDISO <sub>A-B</sub> <sup>(1)</sup>	Floating grounds differential voltage (GNDISO_A - GNDISO_B)		-1700	+1700	V
V <sub>IORM</sub>	Primary to secondary ground (GND - GNDISO_A); (GND - GNDISO_B)		-1200	+1200	V
F <sub>SW</sub>	Maximum switching frequency <sup>(2)</sup>			1	MHz
t <sub>OUT</sub>	Output pulse width		100		ns
T <sub>J</sub>	Operating junction temperature		-40	125	°C

1. Characterization data, 1200 V max. tested in production.
2. Actual limit depends on power dissipation and T<sub>J</sub>.

## 4 Electrical characteristics

**Table 5. Electrical characteristics ( $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{H\_x} = 18\text{ V}$ ,  $V_{DD} = 5\text{ V}$  unless otherwise specified)**

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Dynamic characteristics</b>							
$t_{Don}$	INA, INB, SD, BRAKE	Input to output propagation delay ON	See Figure 8	50	75	90	ns
$t_{Doff}$	INA, INB, SD, BRAKE	Input to output propagation delay OFF	See Figure 8	50	75	90	ns
$t_r$		Rise time	$C_L = 4.7\text{ nF}$ , See Figure 8		30		ns
$t_f$		Fall time			30		ns
MT		Matching time <sup>(1)</sup>				20	ns
$t_{deglitch}$	INA, INB, SD, BRAKE	Inputs deglitch filter			20	40	ns
CMTI <sup>(2)</sup>		Common-mode transient immunity, $ dV_{ISO}/dt $	$V_{CM} = 1500\text{ V}$ , see Figure 9	100			V/ns
<b>Supply voltage</b>							
$V_{H_{on}}$		$V_{H\_x}$ UVLO turn-on threshold		14.6	15.5	16.4	V
$V_{H_{off}}$		$V_{H\_x}$ UVLO turn-off threshold		13.9	14.8	15.7	V
$V_{H_{hyst}}$		$V_{H\_x}$ UVLO hysteresis		600	750	950	mV
$I_{QHU\_A}$ $I_{QHU\_B}$		$V_H$ undervoltage quiescent supply current	$V_H = 7\text{ V}$		1.3	1.8	mA
$I_{QH\_A}$ $I_{QH\_B}$		$V_{H\_x}$ quiescent supply current			1.3	1.8	mA
$I_{QHSBY\_A}$ $I_{QHSBY\_B}$		Standby $V_{H\_x}$ quiescent supply current			400	550	$\mu\text{A}$
SafeClp		GOFF active clamp	$I_{GOFF} = 0.2\text{ A}$ ; $V_H$ floating		2	2.3	V
$I_{QDD}$		VDD quiescent supply current			1.8	2.4	mA
$I_{QDDSBY}$		Standby VDD quiescent supply current	Standby mode		40	80	$\mu\text{A}$
<b>Logic Inputs</b>							
$V_{il}$	INA, INB, SD, BRAKE	High level logic threshold voltage		$0.29 \cdot V_{DD}$	$0.33 \cdot V_{DD}$	$0.37 \cdot V_{DD}$	V
$V_{ih}$	INA, INB, SD, BRAKE	Low level logic threshold voltage		$0.62 \cdot V_{DD}$	$0.66 \cdot V_{DD}$	$0.72 \cdot V_{DD}$	V
$I_{logic\_h}$	INA, INB, SD, BRAKE	Logic inputs high level input bias current	$V_{logic} = 5\text{ V}$	33	50	70	$\mu\text{A}$
$I_{logic\_l}$	INA, INB, SD, BRAKE	Logic inputs low level input bias current	$V_{logic} = 0\text{ V}$			1	$\mu\text{A}$
$R_{pd}$	INA, INB, SD, BRAKE	Logic inputs pull-down resistor		70	100	150	k $\Omega$
<b>Interlocking</b>							
iLOCKen	iLOCK	Interlocking enable voltage		$0.7 \cdot V_{DD}$			V

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
iLOCK <sub>h</sub>	iLOCK	iLOCK high level bias current	iLOCK = VDD			1	μA
iLOCK <sub>l</sub>	iLOCK	iLOCK low level bias current	iLOCK = GND	35	55	75	μA
iLOCK <sub>pu</sub>	iLOCK	iLOCK pull-up resistor		66	90	142	kΩ
<b>Driver buffer section</b>							
I <sub>GON</sub>		Source short-circuit current	T <sub>J</sub> = 25°C		4		A
			T <sub>J</sub> = -40 / +125°C <sup>(2)</sup>	3		5	
V <sub>GONH</sub>		Source output high level voltage	I <sub>GON</sub> = 100 mA	VH-0.15	VH-0.12		V
R <sub>GON</sub>		Source R <sub>DS_ON</sub>	I <sub>GON</sub> = 100 mA		1.25	1.5	Ω
I <sub>GOFF</sub>		Sink short-circuit current	T <sub>J</sub> = 25°C		4		A
			T <sub>J</sub> = -40 / +125°C <sup>(2)</sup>	3		5.5	
V <sub>GOFFL</sub>		Sink output low level voltage	I <sub>GOFF</sub> = 100 mA		110	120	mV
R <sub>GOFF</sub>		Sink R <sub>DS_ON</sub>	I <sub>GOFF</sub> = 100 mA		1.1	1.2	Ω
<b>Miller Clamp</b>							
V <sub>CLAMPth</sub>		CLAMP voltage threshold	V <sub>CLAMP</sub> vs. GNDISO	1.3	2	2.6	V
I <sub>CLAMP</sub>		CLAMP short-circuit current	V <sub>CLAMP</sub> = 15 V				A
			T <sub>J</sub> = 25°C		4		
			T <sub>J</sub> = -40 ÷ +125°C <sup>(2)</sup>	2		5	
V <sub>CLAMP_L</sub>		CLAMP low level output voltage	I <sub>CLAMP</sub> = 100 mA		96	115	mV
R <sub>CLAMP</sub>		CLAMP R <sub>DS_ON</sub>	I <sub>CLAMP</sub> = 100 mA		0.96	1.15	Ω
<b>Overtemperature protection</b>							
T <sub>SD</sub>		Shutdown temperature <sup>(2)</sup>		170			°C
T <sub>hys</sub>		Temperature hysteresis <sup>(2)</sup>			20		°C
<b>Standby</b>							
t <sub>STBY</sub>		Standby time	See Section 6.3	200	280	500	μs
t <sub>WUP</sub>		Wake-up time	See Section 6.3	10	20	35	μs
t <sub>awake</sub>		Wake-up delay	See Section 6.3	90	140	200	μs
t <sub>stbyfilt</sub>		Standby filter	See Section 6.3	200	280	800	ns

1.  $MT = \max(|t_{Don(A)} - t_{Don(B)}|, |t_{Doff(A)} - t_{Doff(B)}|, |t_{Doff(A)} - t_{Don(B)}|, |t_{Doff(B)} - t_{Don(A)}|)$
2. Characterization data, not tested in production.



## 5 Isolation

**Table 6. Isolation and safety-related specifications**

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap )	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index ( Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

**Table 7. Isolation characteristics**

Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum Working Isolation Voltage	$V_{IORM}$		1200	$V_{PEAK}$
Input to Output test voltage In accordance with VDE 0884-11	$V_{PR}$	Method a, Type test	1920	$V_{PEAK}$
		$V_{PR} = V_{IORM} \times 1.6, t_m = 10 \text{ s}$		
		Partial discharge < 5 pC	2250	$V_{PEAK}$
		Method b1, 100 % Production test		
		$V_{PR} = V_{IORM} \times 1.875, t_m = 1 \text{ s}$		
Transient Overvoltage (Highest Allowable Overvoltage)	$V_{IOTM}$	$t_{ini} = 60 \text{ s}$ Type test	6000	$V_{PEAK}$
Maximum Surge Test Voltage	$V_{IOSM}$	Type test	6000	$V_{PEAK}$
Isolation Resistance	$R_{IO}$	$V_{IO} = 500 \text{ V}$ ; Type test	>10 <sup>9</sup>	$\Omega$

**Table 8. Isolation voltage as per UL 1577**

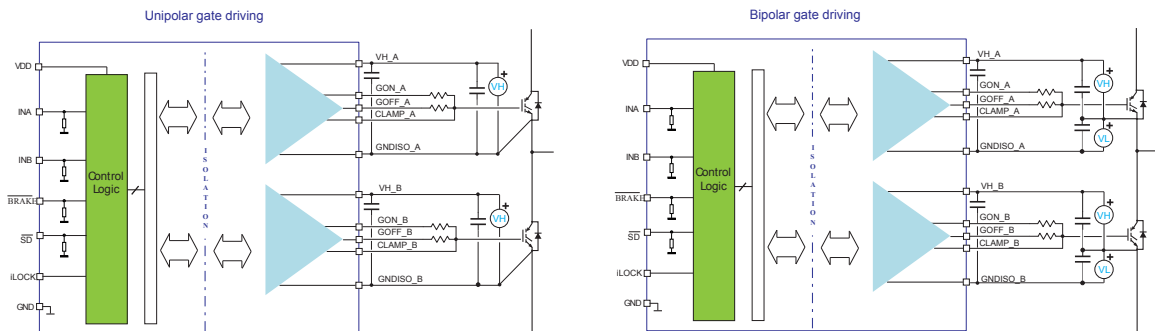
Description	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1min (Type test)	$V_{ISO}$	3535/5000	$V_{rms}/ \text{PEAK}$
Isolation Test Voltage, 1sec (100% production)	$V_{ISOtest}$	4242/6000	$V_{rms}/ \text{PEAK}$

## 6 Functional description

### 6.1 Gate driving power supply and UVLO

The STGAP2SiCD is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows to implement either unipolar or bipolar gate driving.

**Figure 3. Power supply configuration for unipolar and bipolar gate driving**



Undervoltage protection is available on  $VH_x$  supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When  $VH_x$  voltage goes below the  $VH_{off}$  threshold, the output buffer goes into “safe state”. When  $VH_x$  voltage reaches the  $VH_{on}$  threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and  $VH_x$  supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1  $\mu$ F and 10  $\mu$ F should be placed close to it.

### 6.2 Power-up, power-down and ‘safe state’

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance

Such conditions are maintained at power-up of the isolated side ( $VH_x < VH_{on}$ ) and during whole device power-down phase ( $VH < VH_{off}$ ), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when  $VH$  voltage is not high enough to actively turn the internal GOFF MOSFET on. If  $VH_x$  positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side the device output state depends on the input pins' status.

### 6.3 Control Inputs

The device is controlled through the following logic inputs:

- SD: active low shutdown input;
- BRAKE: active low brake input;
- INA, INB: active high logic inputs for channel A and channel B driver outputs;
- iLOCK: used to enable or disable the interlocking protection.

The operation of the driver IOs is described in [Table 9](#).

**Table 9. Inputs truth table (applicable when device is not in UVLO or "safe state")**

	Input pins <sup>(1)</sup>					Output pins	
	iLOCK	SD	BRAKE	INA	INB	GOUT_A	GOUT_B
	X	L	X	X	X	Low	Low
	X	H	L	X	X	Low	<b>HIGH</b>
	X	H	H	L	L	Low	Low
	X	H	H	H	L	<b>HIGH</b>	Low
	X	H	H	L	H	Low	<b>HIGH</b>
<b>Interlocking</b>	VDD	H	H	H	H	Low	Low
	GND	H	H	H	H	<b>HIGH</b>	<b>HIGH</b>

1. X: Don't care

A deglitch filter allows input signals with duration shorter than  $t_{\text{deglitch}}$  to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

### 6.4 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced into "safe state" until communication link is properly established again.

### 6.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the TSD temperature threshold, the device is forced into "safe state". The device operation is restored as soon as the junction temperature is lower than TSD - Thys.

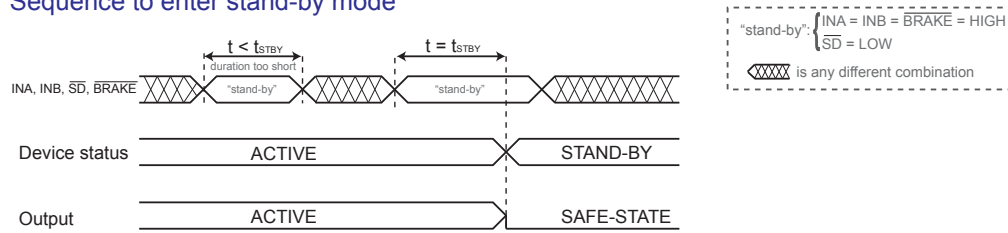
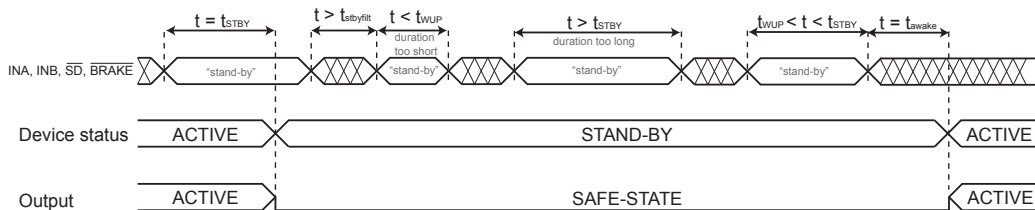
### 6.6 Standby function

In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH\_x supply pins is reduced to  $I_{\text{QDDs}}$  and  $I_{\text{QHS}_x}$  respectively, and the output remains in 'safe state' (the output is actively forced low).

The way to enter standby is to keep the SD low while keeping the other input pins (INA, INB and BRAKE) high ("standby" value) for a time longer than  $t_{\text{STBY}}$ . During standby the inputs can change from the "standby" value.

To exit standby, inputs must be put in any combination different from the "standby" value for a time longer than  $t_{\text{stbyfilt}}$ , and then in the "standby" value for a time  $t$  such that  $t_{\text{WUP}} < t < t_{\text{STBY}}$ .

When the input configuration is changed from the "standby" value the output is enabled and set according to inputs state after a time  $t_{\text{awake}}$ .

**Figure 4. Standby state sequences**
**Sequence to enter stand-by mode**

**Sequence to exit stand-by mode**


## 6.7 Interlocking function

The interlocking function prevents outputs GOUT\_A and GOUT\_B from being high at the same time, regardless of the status of the input pins INA and INB. In half-bridge topologies this protection avoids shoot-through in case wrong input signals are generated by the controller device. If the status of INA and INB is such to require both channels to be ON at the same time, the driver turns both channels off. In some topologies it is required to allow both channels to be ON at the same time: this can be achieved by disabling the interlocking function through the iLOCK pin. The iLOCK pin is either connected to VDD, which enables the interlocking function, or to GND, which disables the interlocking function and allows parallel operation of Channel\_A and Channel\_B. Refer to Control Inputs for complete logic inputs truth table.

## 7 Typical application diagram

Figure 5. Typical application diagram – Half-bridge configuration

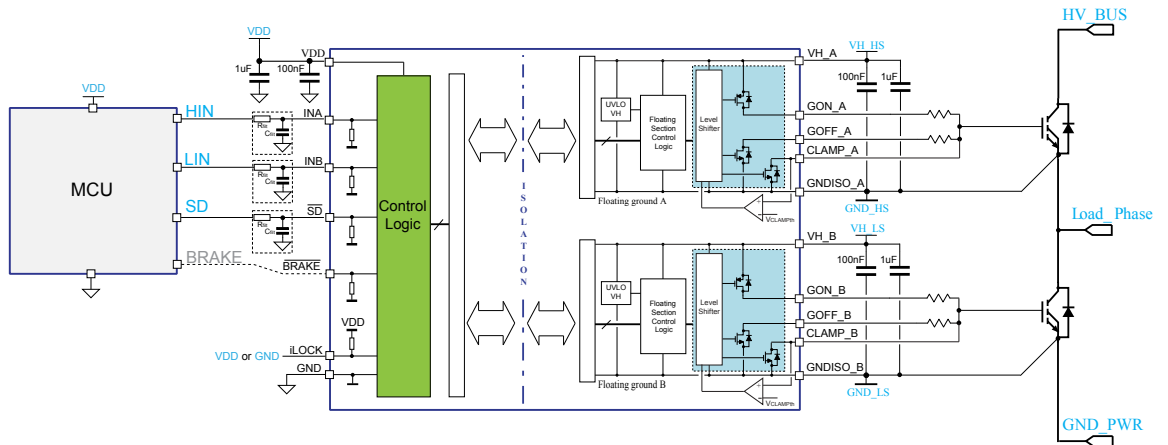
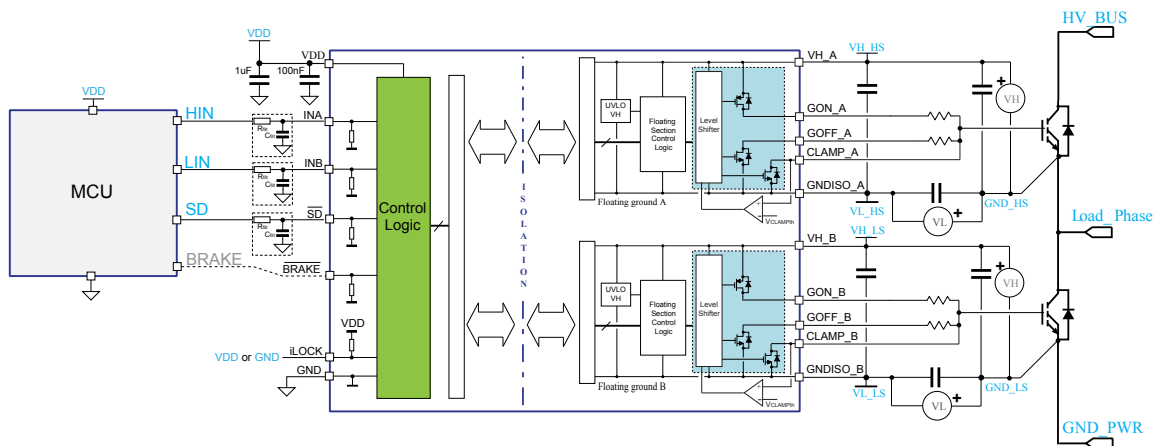


Figure 6. Typical application diagram – Half-bridge configuration with negative gate driving



## 8 Layout

### 8.1 Layout guidelines and considerations

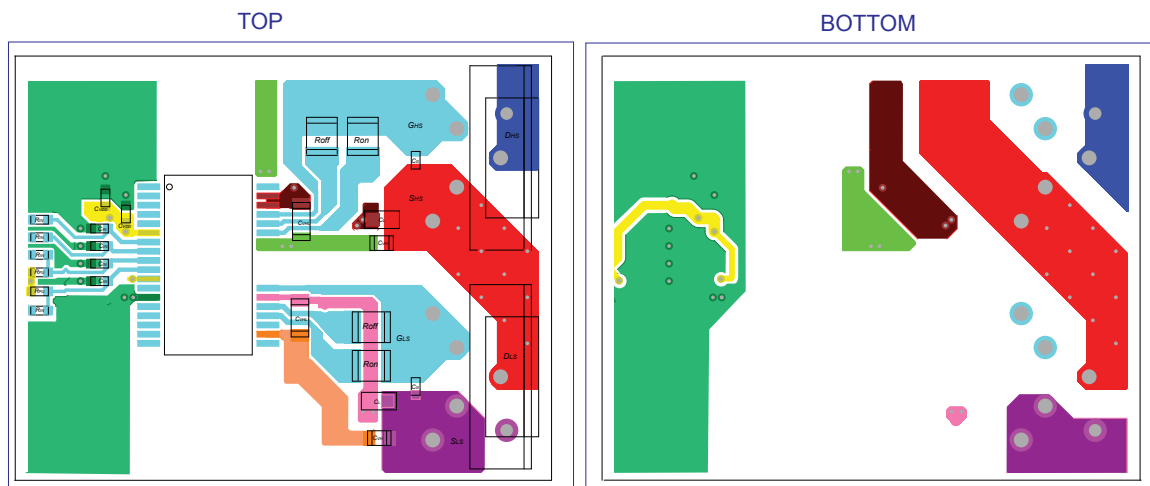
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMD ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF capacitor must be placed between VDD and GND and between VH\_x and GNDISO\_x, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current a second capacitor with value in the range between 1  $\mu$ F and 10  $\mu$ F should also be placed close to the supply pins.
  - As a good practice it is suggested to add filtering capacitors close to logic inputs of the device (INA, INB, BRAKE, SD), in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might cause noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should be no trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH\_x and GNDISO\_x pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

### 8.2 Layout example

An example of STGAP2SiCD suggested half-bridge with negative gate driving PCB layout is shown in [Figure 7](#) ; the main signals have been highlighted by different colors. It is recommended to follow this example for proper positioning and connection of filtering capacitors. It is recommended to follow this example for proper positioning and connection of filtering capacitors.

**Figure 7. Suggested PCB layout for half-bridge configuration with negative driving voltage**



## 9 Testing and characterization information

Figure 8. Timings definition

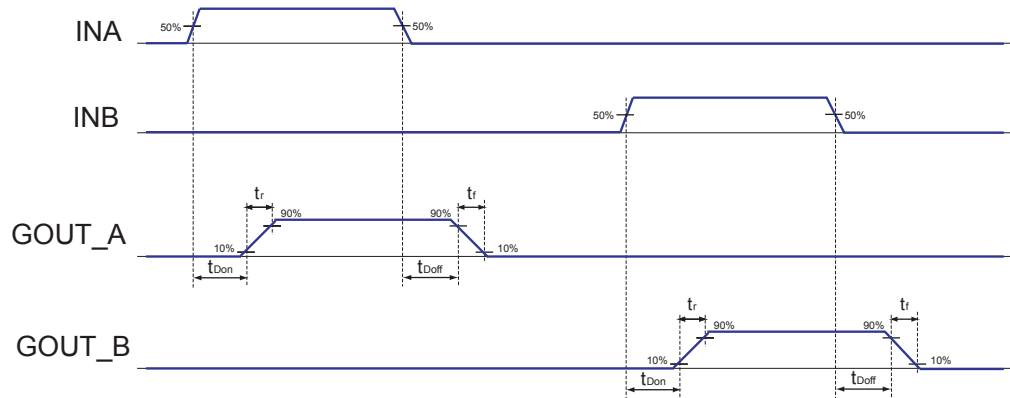
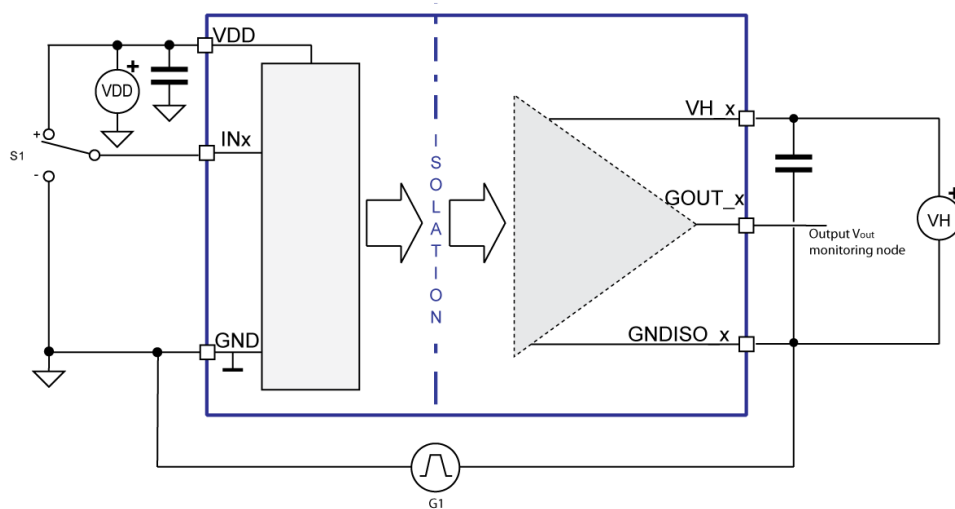


Figure 9. CMTI test circuit



## 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 10.1 SO-36W package information

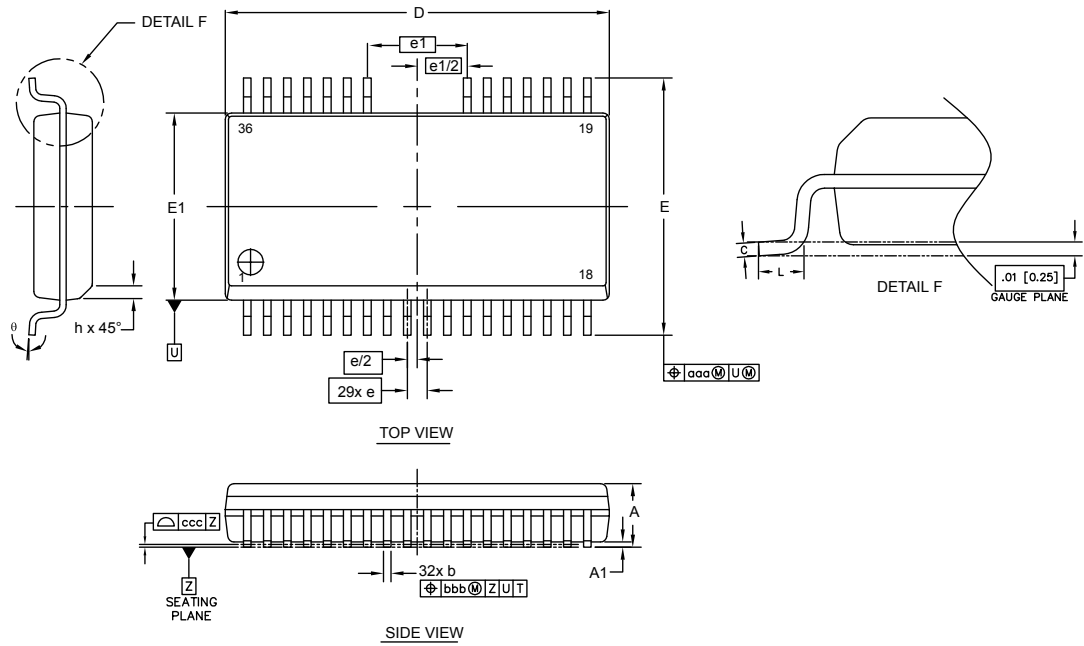
**Table 10. SO-36W package dimensions**

Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs are not to exceed 0.15 mm per side.

Dim.	mm			NOTES
	Min.	Typ.	Max.	
A			2.65	
A1	0.1		0.3	
b	0.25		0.35	
c	0.20		0.33	
D	15.20		15.60	
E1	7.4		7.6	
E	10.05		10.65	
e		0.80		
e1		4.00		
L	0.61		0.91	
h	0.25		0.75	
θ	0°		8°	
aaa		0.25		
bbb		0.25		
ccc		0.10		

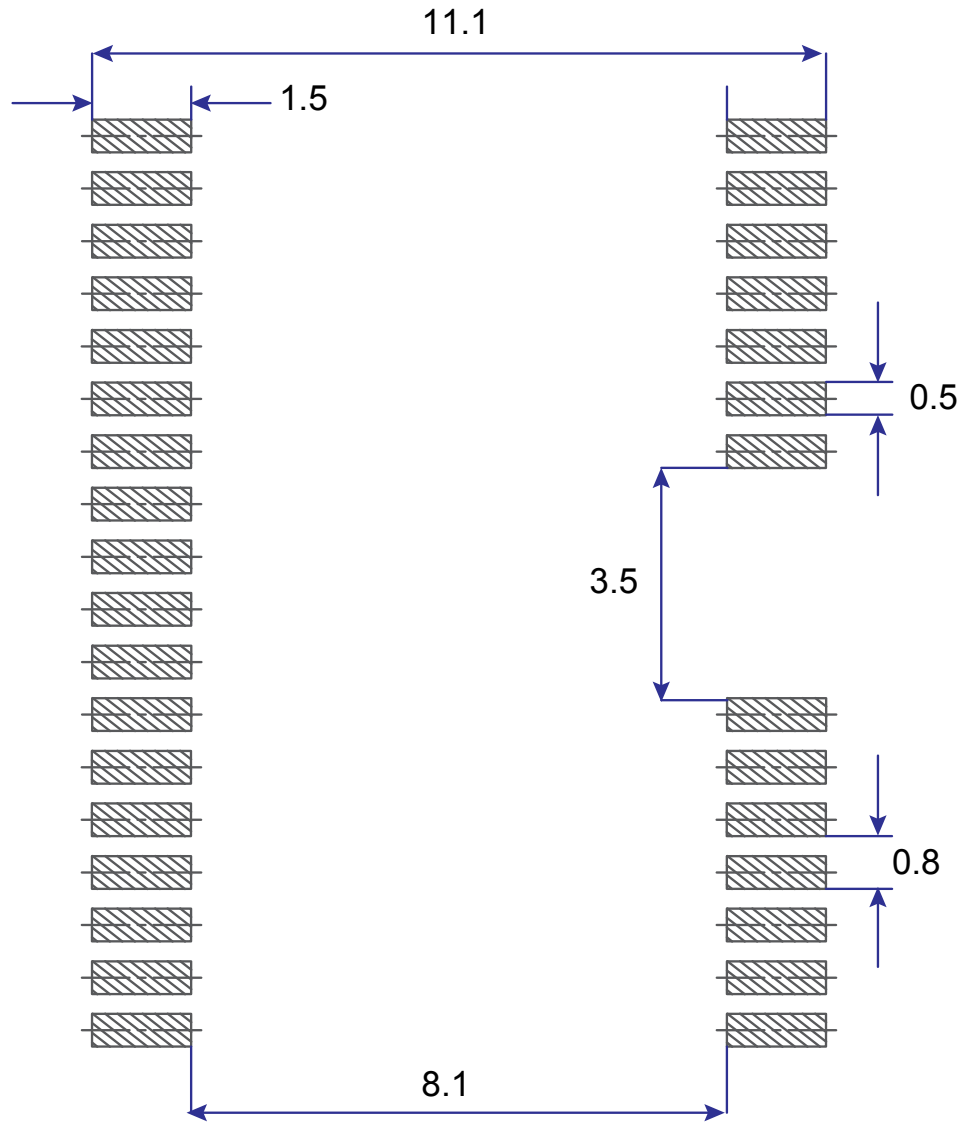


Figure 10. SO-36W package outline



## 11 Suggested land pattern

Figure 11. SO-36W suggested land pattern



## 12 Ordering information

**Table 11. Device summary**

Order code	Output configuration	Package	Package marking	Packaging
<b>STGAP2SiCD</b>	Separated outputs and Miller CLAMP	SO-36W	GAP2ID	Tube
<b>STGAP2SiCDTR</b>	Separated outputs and Miller CLAMP	SO-36W	GAP2ID	Tape and Reel

## Revision history

**Table 12. Document revision history**

Date	Version	Changes
18-Oct-2021	1	Initial release.

## Contents

<b>1</b>	<b>Block diagram</b> .....	<b>2</b>
<b>2</b>	<b>Pin description and connection diagram</b> .....	<b>3</b>
<b>3</b>	<b>Electrical data</b> .....	<b>4</b>
<b>3.1</b>	Absolute maximum ratings .....	4
<b>3.2</b>	Thermal data .....	4
<b>3.3</b>	Recommended operating conditions .....	5
<b>4</b>	<b>Electrical characteristics</b> .....	<b>6</b>
<b>5</b>	<b>Isolation</b> .....	<b>8</b>
<b>6</b>	<b>Functional description</b> .....	<b>9</b>
<b>6.1</b>	Gate driving power supply and UVLO .....	9
<b>6.2</b>	Power-up, power-down and 'safe state' .....	9
<b>6.3</b>	Control Inputs .....	10
<b>6.4</b>	Watchdog .....	10
<b>6.5</b>	Thermal shutdown protection .....	10
<b>6.6</b>	Standby function .....	10
<b>6.7</b>	Interlocking function .....	11
<b>7</b>	<b>Typical application diagram</b> .....	<b>12</b>
<b>8</b>	<b>Layout</b> .....	<b>13</b>
<b>8.1</b>	Layout guidelines and considerations .....	13
<b>8.2</b>	Layout example .....	13
<b>9</b>	<b>Testing and characterization information</b> .....	<b>14</b>
<b>10</b>	<b>Package information</b> .....	<b>15</b>
<b>10.1</b>	SO-36W package information .....	15
<b>11</b>	<b>Suggested land pattern</b> .....	<b>17</b>
<b>12</b>	<b>Ordering information</b> .....	<b>18</b>
	<b>Revision history</b> .....	<b>19</b>
	<b>Contents</b> .....	<b>20</b>
	<b>List of tables</b> .....	<b>21</b>
	<b>List of figures</b> .....	<b>22</b>

## List of tables

<b>Table 1.</b>	Pin description . . . . .	3
<b>Table 2.</b>	Absolute maximum ratings . . . . .	4
<b>Table 3.</b>	Thermal data . . . . .	4
<b>Table 4.</b>	Recommended operating conditions . . . . .	5
<b>Table 5.</b>	Electrical characteristics ( $T_J = 25\text{ }^\circ\text{C}$ , $V_{H\_x} = 18\text{ V}$ , $V_{DD} = 5\text{ V}$ unless otherwise specified) . . . . .	6
<b>Table 6.</b>	Isolation and safety-related specifications . . . . .	8
<b>Table 7.</b>	Isolation characteristics . . . . .	8
<b>Table 8.</b>	Isolation voltage as per UL 1577 . . . . .	8
<b>Table 9.</b>	Inputs truth table (applicable when device is not in UVLO or "safe state") . . . . .	10
<b>Table 10.</b>	SO-36W package dimensions . . . . .	15
<b>Table 11.</b>	Device summary . . . . .	18
<b>Table 12.</b>	Document revision history . . . . .	19

## List of figures

Figure 1.	Block diagram . . . . .	2
Figure 2.	Pin connection (top view) . . . . .	3
Figure 3.	Power supply configuration for unipolar and bipolar gate driving . . . . .	9
Figure 4.	Standby state sequences . . . . .	11
Figure 5.	Typical application diagram – Half-bridge configuration . . . . .	12
Figure 6.	Typical application diagram – Half-bridge configuration with negative gate driving . . . . .	12
Figure 7.	Suggested PCB layout for half-bridge configuration with negative driving voltage . . . . .	13
Figure 8.	Timings definition . . . . .	14
Figure 9.	CMTI test circuit . . . . .	14
Figure 10.	SO-36W package outline . . . . .	16
Figure 11.	SO-36W suggested land pattern . . . . .	17

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