RTL8811AU

SINGLE-CHIP IEEE 802.11b/g/n/ac 1T1R WLAN USB 2.0 CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012/09/05	First release.
1.1	2013/04/09	1.) Delete EEPROM description 2.) Delete USB_FUN_SEL pin 3.) VIO_UART replace to VDIO 4.) EEPROM_SEL replace to NV_SELn

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1. General Description

The Realtek RTL8811AU is a highly integrated single-chip IEEE 802.11b/g/n/ac 1T1R USB2.0 WLAN controller. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip. The RTL8811AU provides a complete solution for a high throughput performance integrated wireless LAN and Bluetooth device.

The RTL8811AU WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the IEEE 802.11ac specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz , 40MHz and 80MHz channel bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256-QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 433.3Mbps for IEEE 802.11ac OFDM.

A RTL8811AU built-in enhanced signal detector, adaptive frequency domain equalizer, and a soft-decision Viterbi decoder help to alleviate multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8811AU WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain better performance in the analog portions of the transceiver.

The RTL8811AU WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n/802.11ac Draft 2.0 for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensate for the extra power required to transmit OFDM. The RTL8811AU provides simple legacy and 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 56-pin QFN
- IEEE 802.11b/g/n/ac Draft 3.0 1T1R WLAN and Bluetooth single chip

Host Interface

- Complies with USB2.0 for WLAN controller

WLAN Controller

- CMOS MAC, Baseband PHY, and RF in a single chip for IEEE 802.11b/g/n/ac Draft 3.0 compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- 433.3Mbps receive PHY rate and 433.3Mbps transmit PHY rate using 80MHz bandwidth
- Backward compatible with 802.11b/g devices while operating in 802.11n mode
- IEEE 802.11b/g/n/ac Draft 3.0 compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Multi MACID support with Fast Channel switch
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications

WLAN PHY Features

- IEEE 802.11n/ac OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz, 40MHz and 80MHz bandwidth transmission
- Support 2.4GHz and 5GHz band channels
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble

- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in IEEE 802.11g; and 150Mbps in IEEE 802.11n; and 433.3Mbps in IEEE 802.11ac
- Switch diversity for DSSS/CCK
- Packet based hardware antenna diversity
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Integrated 2.4G/ 5G CMOS PA

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- CCA on secondary through RTS/CTS handshake
- Support TCP/UDP/IP checksum offload

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- Three configurable LED pins
- Flexible XTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support XTAL or external clock input

3. Application Diagram

3.1. Dual-Band 11ac (1x1) Solution with Single Antenna

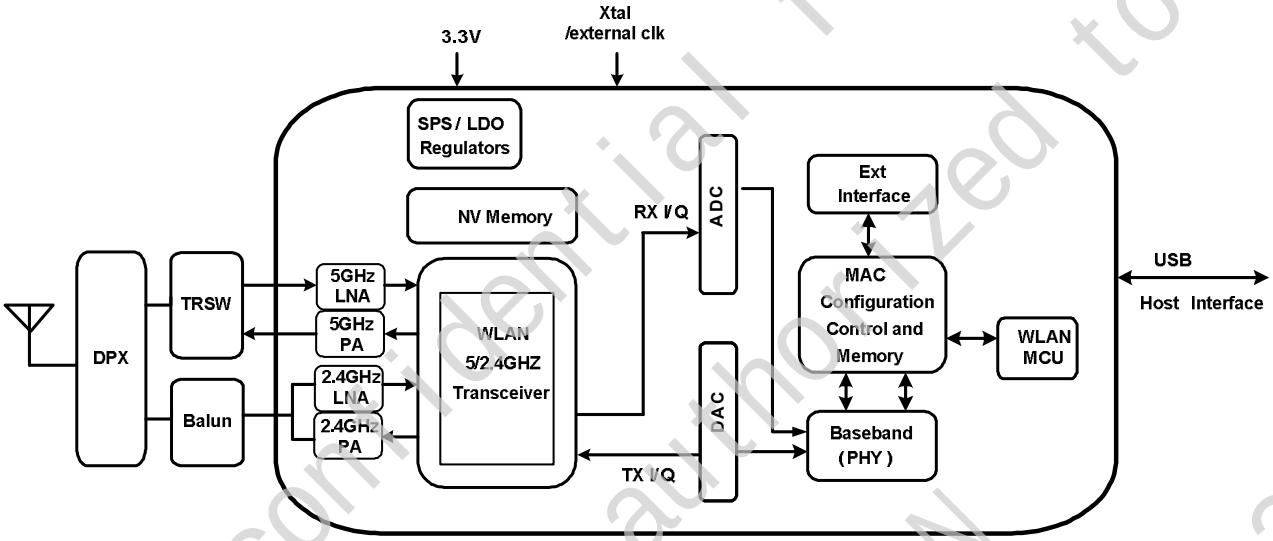


Figure 1. Dual-Band 11ac (1x1) Solution with single Antenna

3.2. Dual-Band 11ac (1x1) Solution Antenna Diversity

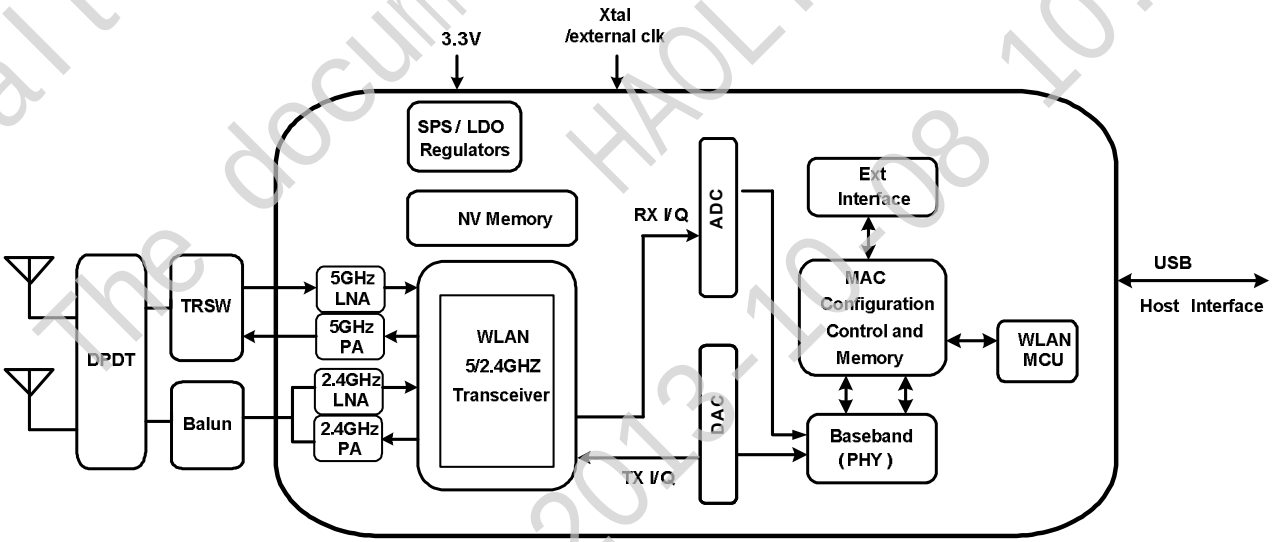


Figure 2. Dual-Band 11ac (1x1) Solution with Antenna Diversity

Pin Assignments

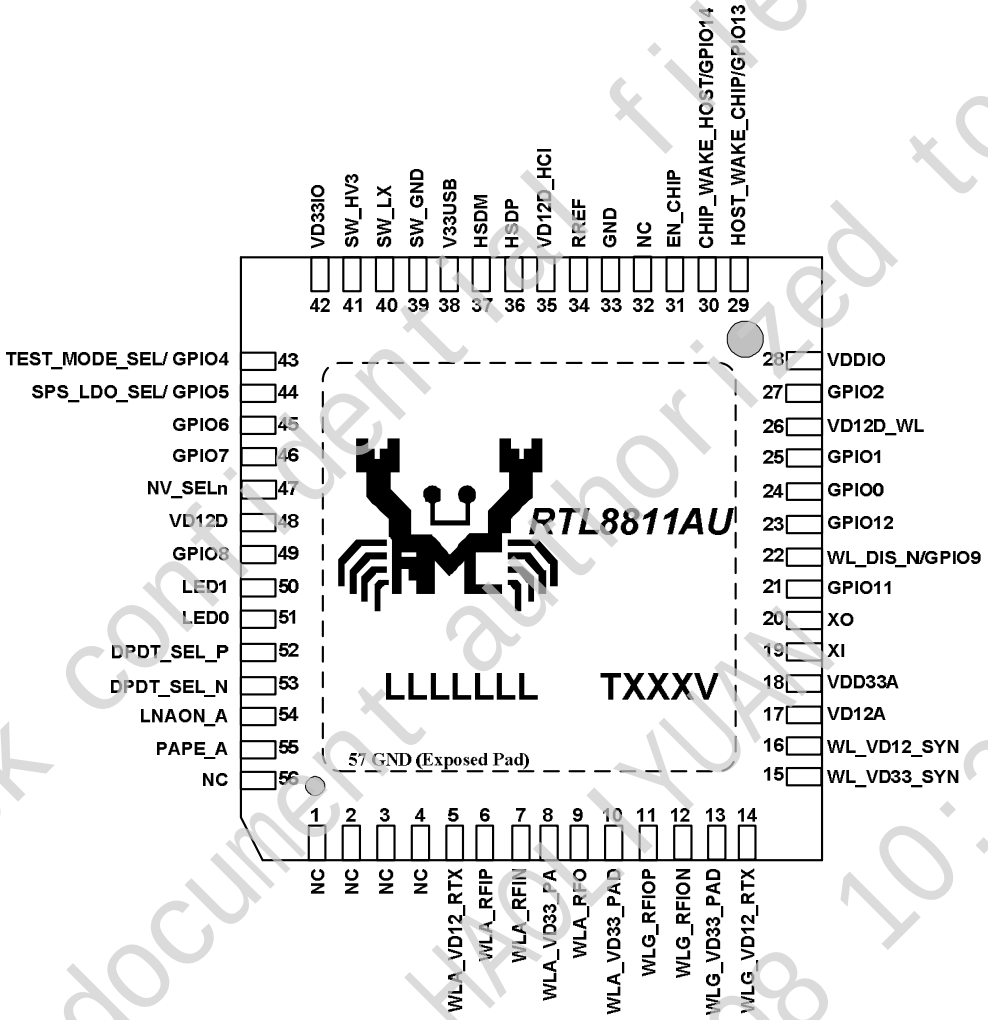


Figure 3. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 3.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

5.1. Power-On Trap Pins

Table 1. Power On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	43	0: Normal operation mode 1: Enter into test/debug mode
SPS_LDO_SEL	I	44	0: Internal switching regulator select 1: Internal LDO select
NV_SELn	I	47	0: Internal NV memory select

5.2. USB Transceiver Interface

Table 2. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP	IO	36	High-Speed USB D+ Signal
HSDM	IO	37	High-Speed USB D- Signal

5.3. RF Interface

Table 3. RF Interface

Symbol	Type	Pin No	Description
WLA_RFI	I	6, 7	WL 5GHz RF RX signal
WLA_RFO	O	9	WL 5GHz RF TX signal
WLG_RFIOP	IO	11	WL 5GHz RF TRX positive signal
WLG_RFION	IO	12	WL 5GHz RF TRX negative signal
PAPE_A	O	55	RF external components control signal
LNAON_A	O	54	RF external components control signal
DPDT_SEL_N	O	53	RF external components control signal
DPDT_SEL_P	O	52	RF external components control signal

5.4. LED Interface

Table 4. LED Interface

Symbol	Type	Pin No	
LED0	O	51	LED pins
LED1	O	50	LED pins
GPIO8	O	49	LED pins Shared with GPIO8, can be selected by control register

5.5. Power Management Handshake Interface

Table 5. Power Management Handshake Interface

Symbol	Type	Pin No	Description
EN_CHIP	I	31	enable chip
WL_DIS_N/ GPIO9	I	22	This Pin Can Externally Shutdown the RTL8811AU (no requirement for Extra Power Switch) when WL_DISn is pulled low and GPIO11 is also pulled low.
GPIO12/WPS	I	23	This pin can be detected by WIFI controller to initiate WPS procedure
HOST_WAKE_CHIP/ GPIO13	I	29	Host wakeup chip pin
CHIP_WAKE_HOST/ GPIO14	O	30	chip wakeup host pin

5.6. Clock and Other Pins

Table 6. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	19	reference OSC input reference crystal input
XO	O	20	reference crystal output external clock input

5.7. Power Pins

Table 7. Power Pins

Symbol	Type	Pin No	
WLA_VD12_RTX	P	5	1.2V for WLA RF
WLA_VD33_PA	P	8	3.3V for WLA PA
WLA_VD33_PAD	P	10	3.3V for WLA PA driver
WLG_VD33_PAD	P	13	3.3V for WLG PA driver
WLG_VD12_RTX	P	14	3.3V for WLG RF
WL_VD33_SYN	P	15	3.3V for WL synthesizer
WL_VD12_SYN	P	16	1.2V for WL synthesizer
VD12A	P	17	1.2V for WL AFE
VDD33A	P	18	3.3V for WL AFE
VD33IO	C	42	3.3V GPIO IO power
SW_HV3	P	41	Switching regulator input
SW_LX	P	40	Switching regulator output
SW_GND	G	39	Ground for switching regulator
VD12D	P	48	digital power
VD12D_WL	P	26	1.2V for WL digital power
VDDIO	P	28	GPIOs IO power
V33_USB	P	38	supply voltage for USB IO

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. Power Supply DC Characteristics

Table 9. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
WLA_VD33_PA, WLA_VD33_PAD, WLG_VD33_PAD, WL_VD33_SYN, VD33IO, SW_HV3, V33USB, VD33A	3.3V I/O and RFAFE Supply Voltage	3.0	3.3	3.6	V
WLG_VD12_RTX, VD12D, WL_VD12_SYN, VD12A, VD12D_WL, VD12D_HCI	1.2V Core and RFAFE Supply Voltage	1.10	1.2	1.32	V
IDD33	3.3V Rating Current	-	-	600	mA

6.3. Digital IO Pin DC Characteristics

Table 10. 3.3V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	-	0	0.9	V
V_{OH}	Output high voltage	2.97	-	3.3	V
V_{OL}	Output low voltage	0	-	0.33	V

6.4. USB Bus during Power On Sequence

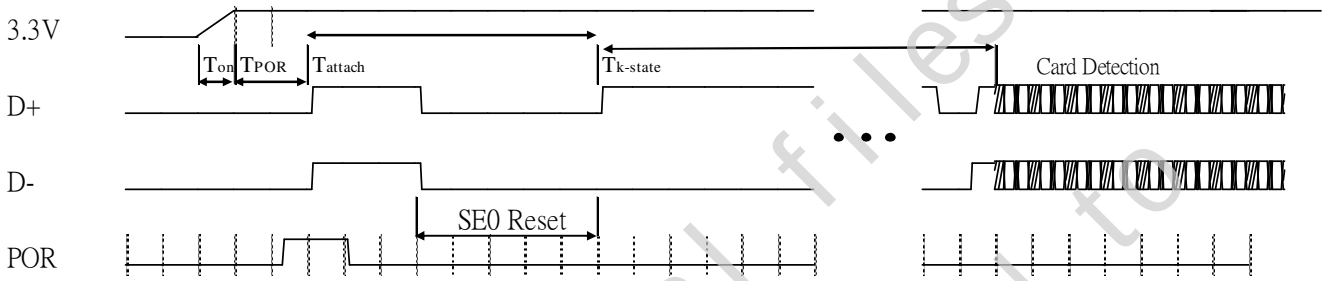


Figure 4. RTL8811AU USB Bus Power On Sequence

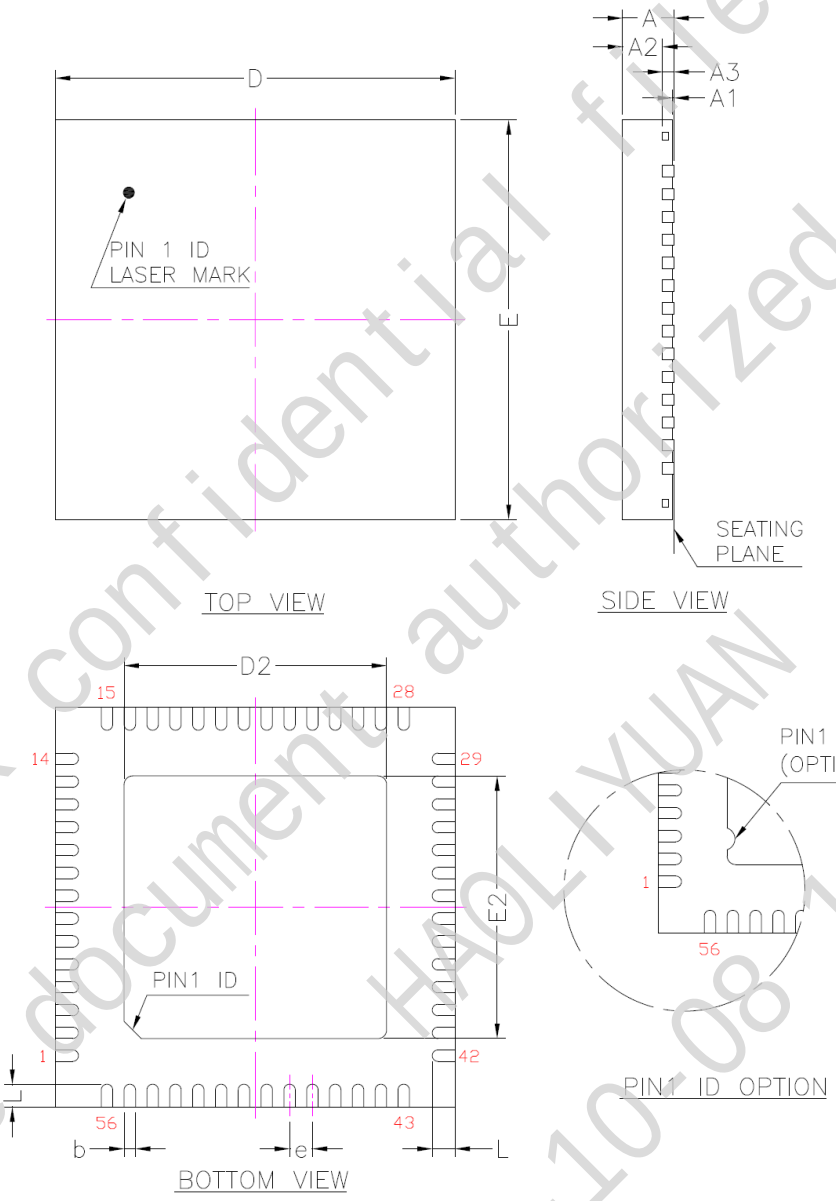
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state
$T_{k\text{-}state}$: the duration from resister attached to USB host starting card detection procedure

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 11. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	--	1.5	5
T_{por}	ms	--	2	10
T_{attach}	ms	2	7	15
$T_{k\text{-}state}$	ms	50	250	--

7. Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3		0.2 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		7.00 BSC			0.276 BSC	
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

Ordering Information

Table 12. Ordering Information

Part Number	Package	Status
RTL8811AU-CG	QFN-56, 'Green' Package	Mass Production

Note: See page 6 for package identification.

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